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Germanium and Epitaxial Ge:C Devices for CMOS Extension and Beyond

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Germanium and Epitaxial Ge:C Devices for CMOS Extension and Beyond

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Dedication

To my parents

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Germanium and Epitaxial Ge:C Devices for CMOS Extension and Beyond

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Supervisor: Sanjay K. Banerjee

This work focuses on device design and process integration of high-performance Ge-based devices for CMOS applications and beyond. Here we addressed several key challenges towards Ge-based devices, such as, poor passivation, underperformance of nMOSFETs, and incompatibility of fragile Ge wafers for mass production.

We simultaneously addressed the issues of bulk Ge and passivation for pMOSFETs, by fabricating Si-capped epitaxial Ge:C(C<0.5%) devices. Carbon improves the crystalline quality of the channel, while Si capping prevents GeO_x formation, creates a quantum well for holes and thus improves mobility. Temperature-dependent characterization of these devices suggests that Si cap thickness needs to be optimized to ensure highest mobility.

We developed a simple approach to grow GeO_2 by rapid thermal oxidation, which provides improved passivation, especially for nMOSFETs. The MOSCAPs with GeO_2 passivation show ~10× lower D_{it} (~8×10^{11} $cm^{-2}eV^{-1}$) than that of the HF-last devices. The

Ge (111) nMOSFETs with GeO_2 passivation show ~2× enhancement in mobility (~715 $cm^2V^{-1}s^{-1}$ at peak) and ~1.6× enhancement in drive current over control Si (100) devices.

For improved n^+/p junctions, we proposed a simple technique of rapid thermal diffusion from "spin-on-dopants" to avoid implantation damage during junction formation. These junctions show a high I_{ON}/I_{OFF} ratio (~10^{5-6}) and an ideality factor of ~1.03, indicating a low defect density, whereas, ion-implanted junctions show higher I_{off} (by ~1-2 orders) and a larger ideality factor (~1.45). Diffusion-doped and GeO_2-passivated Ge(100) nMOSFETs show a high I_{ON}/I_{OFF} ratio (~10^{4-5}) , a low SS (111 mV/decade), and a high μ_{eff} (679 $cm^2V^{-1}s^{-1}$ at peak). Moreover, diffusion-doped Ge (111) nMOSFETs show even higher μ_{eff} (970 $cm^2V^{-1}s^{-1}$ at peak) that surpasses the universal Si mobility at low E_{eff}.

For Beyond CMOS devices, we investigated Mn-doped Ge:C-on-Si (100), a novel Si-compatible ferromagnetic semiconductor. The investigation suggests that the magnetic properties of these films depend strongly on crystalline structure and Mn concentration. On a different approach, we developed LaO_x/SiO_x barrier for Spin-diodes that reduces contact resistance by ~10^4, compared to Al_2O_3 controls and hence is more conducive for spin injection. These ferromagnetic materials and devices can potentially be useful for novel spintronic devices.

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Chapter 1: Introduction

1.1 CMOS SCALING

Since the beginning of CMOS industry, performance enhancement in integrated circuits has been governed by the famous "Moore's law", which suggests that to ensure a steady economic return, the number of transistors in a given area on Si needs to be doubled in every new technology node [1] (Figure 1.1). Therefore, in every new node, in order to maintain this scaling goal, the MOSFET channel lengths need to be shrunk down to ~70% of their previous lengths. Similarly, other device parameters, such as doping density, capacitance etc., also need to be scaled accordingly to maintain a reliable and predictable behavior in the devices from node to node [2]. To ensure this continuity, semiconductor industry has adopted a standard approach for scaling, popularly known as the "Denard's law" that relies on the principle of maintaining a constant field in the devices from one generation to the next [3] (Figure 1.2). The benefits of such scaling are twofold. In addition to the obvious gain in Si real estate, such physical scaling also improves circuit performance in terms of faster operations, as the smaller and densely packed transistors switch faster because of their higher current density and or shorter time delay [4]. However, as the device channel length and the pitch between the devices are getting smaller and smaller, such physical scaling are getting more and more challenging for numerous reasons. Among them, limitations in optical lithography [5, 6] and etch technology [7] are probably the most critical that determine the minimum possible feature size. From electrical design perspective, the higher channel doping required, increased GIDL, inadequate control of short channel effects, increased parasitics, such as, series resistance and fringing capacitance in shorter channel devices pose significant challenge towards further physical scaling of CMOS devices [8]. As a result, performance enhancement from mere physical scaling is not as high as expected, especially in recent

aggressively scaled technology nodes. Therefore, in addition to physical scaling, several synergistic approaches (Figure 1.3) are being investigated and employed to enhance the performance of sub-100 nm CMOS devices and beyond [9],[10]. Among these approaches, high-k dielectrics have been introduced to reduce the equivalent oxide thickness (EOT) of the gate stack, while maintaining a low leakage current density [11]. Novel 3D architecture and Si-on-insulator substrates will soon be introduced to improve electrostatic control [12]. Last but not least, in recent technology nodes, strain engineering has been arguably the most instrumental of these performance scaling approaches, which improves the drive current of the devices by increasing the channel mobility, and hence assists to maintain the Moore's law [13]. However, as the pitch between the devices is getting smaller with continuous physical scaling, the performance gain from conventional strain engineering is also getting smaller. For instance, as the pitch between the nMOSFETs gets smaller, the Si_3N_4 liner deposited on them gets pinched-off and loses its characteristic shape responsible for providing strain, which results in lower tensile strain in the channel. Similarly, as the volume of the recessed $Si_{1-x}Ge_x$ S/D stressors are getting smaller, effective compressive strain in the channel is also getting smaller and so does the hole mobility enhancement [14]. Consequently, as shown in figure 1.4, performance gain from these traditional strain engineering techniques will soon be reaching a point of diminishing returns.

1.2 MOTIVATION FOR Ge-BASED CMOS DEVICES

As the physical limits of scaling are on the horizon and conventional strain engineering techniques are reaching a point of diminishing returns, novel channel materials with high intrinsic mobility are receiving immense interest [15]. Several semiconductors, such as, Ge, GaAs, InP, InSb, etc. are attractive as channel materials for their high electron or hole mobilities. The key physical properties of these materials are summarized in Table 1. Among these novel materials, Ge has drawn huge interest from

the semiconductor industry because of its high intrinsic hole and electron mobility, smaller bandgap and lower processing temperature. Germanium has ~4× higher hole mobility and ~2× higher electron (e^-) mobility than that of Si, whereas, GaAs and other III-V semiconductors show low hole mobility, even lower than that of Si. Besides, the density of states for both holes and electrons are lower in III-V semiconductors than that of Ge [16]. The lower density of states may cause a lower drive current in aggressively scaled devices (eg. EOT ~0.5 nm), despite their higher intrinsic mobility [17] . Moreover, Ge is also more attractive from the perspective of high volume semiconductor manufacturing as epitaxial Ge can be deposited using CVD systems with high throughput. Besides, like Si, Ge is a non-polar column IV material and hence is more compatible with current Si technology. Furthermore, Ge is already in use in the state-of-the-art integrated circuits, in the form of $Si_{1-x}Ge_x$ stressors in the S/D regions [18].

1.3 CHALLENGES TOWARDS Ge-BASED CMOS

On the other hand, like any other new technology, Ge has its own shortcomings (Figure 1.5) and hence despite all its advantages, introduction of Ge as a channel material in high volume CMOS manufacturing requires extensive process development [19]. Among these shortcomings, lack of a stable native oxide, underperformance of Ge nMOSFETs, and incompatibility of bulk Ge wafers for high volume production are presumably among the major demerits of Ge.

1.3.1 Surface Passivation of Ge

Native GeO_2 is water soluble and very unstable, hence GeO_2/Ge systems cannot be used as a straightforward analog of SiO_2/Si system [16]. Recent developments in high-k technology suggest that high-k dielectrics may be used as an alternative to the Ge-based oxides to fabricate high performance Ge devices. However, the direct deposition of high-k dielectrics on Ge results in a high interface-state density (D_{it}) [16, 19]. In order to reduce D_{it} at the Ge/high-k interface, researchers around the world are searching for

passivation schemes suitable for Ge [20-23]. Some of these passivation schemes were instrumental to fabricate Ge pMOSFETs (Si[24], Al_2O_3[25], AlN[26], CeO_2[27] etc.) that demonstrated high hole mobility. Among these schemes, Si capping layer seems to be very effective to prevent GeO_x formation and to passivate the Ge surface. Besides, the Si cap also creates a quantum well for holes in the Si/Ge:C/Si structure[28]. As a result of this quantum well structure, in addition to providing surface passivation, Si cap is also expected to enhance the Ge pMOSFET performance by reducing remote Coulomb scattering from the traps in the high-k dielectric and surface roughness scattering at the dielectric/semiconductor interface. The Si cap should be thick enough to ensure the above mentioned advantages. However, if it is too thick, gate control becomes weaker as capacitance goes down and channel may form in the second subband in the lower mobility Si cap, especially at higher inversion charge densities. Moreover, because of the lattice mismatch between Ge and Si, thicker Si caps are prone to misfit dislocations that may cause charge trapping and degrade the device performance severely [29, 30]. Hence, in order to achieve the best performance from Si-capped Ge pMOSFETs, Si cap thickness needs to be critically optimized for better passivation and higher mobility, while maintaining a good electrostatic control.

1.3.2 Underperformance of Ge nMOSFETs

Although some passivation schemes (Si[24],Al_2O_3[25], AlN[26], CeO_2[27] etc.) resulted in high hole mobility in Ge pMOSFETs, Ge nMOSFETs fabricated using similar schemes show much lower inversion channel mobility than their Si counterparts (Si[24],Al_2O_3[25], AlN[26], CeO_2[27] etc.), in spite of the higher intrinsic electron mobility of Ge. Therefore, another major challenge towards the realization of Ge-based CMOS is to understand and overcome the causes for such underperformance in Ge nMOSFETs.

Passivation for nMOSFETs

Lately, the low mobility observed in historic Ge nMOSFETs fabricated using conventional passivation schemes has been attributed to the high interface state density (D_{it}) near the conduction band (CB) edge[31] [32]. However, there are only a few recent passivation schemes using GeO_2-based gate dielectrics (e.g. by ozone oxidation [33], molecular beam epitaxy [34], high pressure oxidation[35] etc.), which showed low D_{it}, especially near the CB edge[33] and hence are promising for nMOSFET applications. However, extensive process development is required for CMOS integration of GeO_2-based passivation techniques, as GeO_2 is water-soluble and thermally unstable[36]. Besides, although the effective electron mobility achieved in the GeO_2-passivated devices in this work and by several other groups [34, 37] is higher than that of the devices without GeO_2, the enhancement in mobility is not as high as expected. Moreover, in general, Ge nMOSFETs also suffer from a high off-state junction leakage [34, 38]. Therefore, a careful investigation of GeO_2-passivated nMOSFETs is necessary to gain further insight on the reasons for underperformance of Ge nMOSFETs.

Germanium n^+/p junctions

In addition to surface passivation, another major roadblock towards fabrication of high performance Ge-based nMOSFETs is the poor quality of n^+/p junctions. Although GeO_2 grown by different approaches show promise as a passivation scheme for nMOSFETs [39, 40], realization of good n^+/p junctions in Ge still remains challenging [38, 40, 41]. The low I_{ON} in Ge devices is attributed to the low activation in the n^+ regions due to low solid solubility and fast diffusion of n-type dopants in Ge [38] . Besides, most of the Ge n^+/p junctions reported in literature are fabricated by ion implantation and the underperformance of these n^+/p junctions is also attributed in part to the inadequate removal of implantation damage [38]. The residual implantation defects may also be responsible for the high I_{OFF} observed in Ge nMOSFETs [42]. Besides, they can also

degrade μ_{eff} due to charge trapping near the junctions [43]. Other than implantation, there are a few alternative approaches to form n^+/p junctions in Ge. For instance, solid source diffusion (SSD) was proposed as a technique to avoid fast diffusion of dopants by avoiding the implantation damage during junction formation[44]. Recently, in situ doping [45] and gas-phase doping[46] were reported as alternative doping techniques that resulted in improved junction characteristics and thus showed importance of fabricating low defect density junctions for Ge nMOSFETs.

1.3.3 Epitaxial Ge for high volume CMOS production

Lastly, bulk Ge wafers are not suitable for high volume CMOS production because of their cost, fragility and poor thermal conductivity. To overcome these issues with bulk Ge, different approaches are being investigated extensively to integrate the high mobility Ge channel on Si substrate by growing epitaxial Ge on Si substrates [47, 48]. However, it is also challenging to grow device quality Ge on Si because of the large lattice mismatch of 4.2% between Ge and Si [49]. A few techniques have been reported that reduce extended defects in epitaxial Ge grown on Si, mostly on Si (100) substrates, yet such techniques typically involve complicated steps including growth of thick buffer layers of graded $Si_{1-x}Ge_x$, cyclic H-annealing [50], chemical mechanical polishing (CMP), etc. Surfactant-mediated-epitaxy (SME) has been explored to grow relatively smooth Ge films on Si substrates [51], however, typical surfactants (e.g., Sb) may leave unwanted dopants in the grown epitaxial layer [52]. Recently, our group has demonstrated a simpler technique of adding trace amount of C that significantly improves the quality of Ge films grown on Si (100). Besides, fabrication of Ge-on-Insulator substrates is also receiving interest as they simultaneously provide high volume manufacturability and improved electrostatic control [53, 54].

1.4 BEYOND CMOS APPLICATIONS

While high mobility devices are being investigated as a short-term solution for CMOS scaling, spintronic devices are also receiving interest, as a long-term potential alternative to contemporary CMOS devices. Spintronic devices are promising for scaling because of the following reasons. Manipulation of spin states, along with electronic current flow, may provide one additional degree of freedom. Furthermore, these devices are also promising for faster and low power applications [55-57]. Among the proposed spintronic devices, Spin-MOSFET (Figure 1.6) is one of the most attractive structures from the perspective of CMOS integration [58]. Ideally, the S/D regions of these Spin-MOSFETs need to be fabricated using ferromagnetic semiconductors, while the channel formed with dilute magnetic semiconductors [59] may provide additional advantages.

1.4.1 Dilute magnetic semiconductors

Over the last two decades, pioneering research has been performed on dilute magnetic semiconductors (DMS). Among them, (Ga,Mn)As and (In,Mn)As are probably the most studied. The origin of magnetism in these III-V based materials is now fairly well understood as carrier-mediated ferromagnetism [60] which makes them promising for electrically tunable devices. Epitaxial (Ga,Mn)As layers grown by molecular beam epitaxy (MBE) have shown ferromagnetism for Mn concentrations as low as 1% to about 12%. The Curie temperature (T_C) of this material system is found to be a linear function of the effective Mn concentration from as low as about 10 K to about 180 K [60]. Structural analysis of (Ga,Mn)As shows that the Mn ions can occupy two sites within the GaAs lattice. The majority of Mn atoms substitute Ga sites and other Mn atoms are at interstitial sites. The Mn_{Ga} atoms have a total angular momentum of S=5/2 and act as shallow acceptors. The Mn atoms at interstitial sites on the

other hand act as double donors. Ferromagnetism is observed when the impurity band merges with the valence band as then these impurity states become delocalized. At this Mn concentration level, the interaction between local Mn atoms is mediated by the holes in the valence band. Since this magnetic interaction is carrier mediated, it can be modulated by a number of different techniques such as gate voltage, doping, photo-excitation, and band structure engineering and hence these materials are promising for many new technologies, including spintronics, quantum computation, etc [60]. The main challenge with these DMS materials is their low T_C (< 180K). Recently, Mn-doped Ge systems have also drawn attention as an alternative to III-V based DMS because of their Si compatibility [61-63]. In addition, some Ge:Mn systems showed ferromagnetism near or above room-temperature in the forms of Ge:Mn nanowires [64], nanocolumns [65] or nanodots [66], whereas bulk or thick layers of Ge:Mn systems show much lower T_C [61-63, 78-80][i]. Interestingly, it seems that structural confinement may play a role to increase T_C of these Ge:Mn systems.

1.4.2 Ferromagnetic metal/Semiconductor spin-diodes

Another promising approach for fabricating spin-MOSFETs is to integrate ferromagnetic metals with intrinsically high T_C, such as Ni, Fe or Co as the S/D of the devices. Presumably, the biggest challenge of this approach is the contact resistance (R_c) mismatch between the ferromagnetic metals and n-type semiconductors due to the high Schottky barrier or Fermi level pinning between them. The R_c needs to be carefully optimized for efficient spin injection/detection [67]. Several groups are searching for an approach to reduce R_c to fabricate spin-devices on conventional semiconductors using different tunnel barriers [68] or low workfunction ferromagnetic metals [69]. Among them many groups have

[i] Part of this paragraph is adapted with permission from [78], © 2011 by American Physical Society.

demonstrated conceptual spin-devices using different tunnel barriers, ferromagnetic metals and semiconductor substrates [69-71]. However, in general, the operating temperatures of these devices are much lower than that required for realistic use (<<300K), as the R_c is still very high or the T_C of the low workfunction metals are low (eg. 293K for Gd). Therefore, significant process development/design improvement is still required to achieve the ideal R_c for efficient spin-injection [69, 72].

1.5 OUTLINE OF THE DISSERTATION

In the first part of this work, a few synergistic approaches have been investigated to circumvent the above mentioned challenges towards fabrication of high-performance Ge-based CMOS. In the second part of this work we have developed and investigated a novel Si-compatible ferromagnetic semiconductor, and a novel bilayer tunnel barrier for spintronic applications. In the following subsections, the outline of this dissertation is described in brief.

1.5.1 Epitaxial Si/Ge:C/Si buried channel pMOSFETs

In chapter 2, we simultaneously address the issues of bulk Ge and surface passivation, by fabricating Si-capped Ge:C devices on epitaxial Ge:C-on-Si substrates. Epitaxial Ge:C was chosen over epitaxial Ge, as Ge:C shows ~2-3 orders of magnitude lower threading dislocation density (TDD ~ $3\times10^5/cm^2$) than that of epitaxial Ge grown directly on Si substrates [73, 74]. The Si capping layer was deposited in situ to prevent GeO_x formation, to passivate the Ge:C surface and to create a buried channel in the higher mobility Ge:C. The effects of Si cap thickness (3 to 9 nm) on these Ge:C devices have been investigated via temperature-dependent electrical characterization, along with device simulations, which show electrical properties such as drive current, off-state leakage, sub-threshold slope, effective hole mobility, and I_{on}/I_{off} ratio depend strongly on Si cap

thickness and operating temperature. The characterization performed provides us with insights about how to design the optimal Si cap thickness for epitaxial Ge-channel pMOSFETs to achieve high mobility [75].

1.5.2 GeO_2-based surface passivation by rapid thermal oxidation

In Chapter 3, we describe development of a simple route to passivate Ge surface using a thin GeO_2 passivation layer grown by rapid thermal oxidation (RTO). We fabricated $TaN/Al_2O_3/GeO_2/Ge$ MOS capacitors (MOSCAPs) that show improved electrical characteristics over the MOSCAPs without GeO_2. In addition, this chapter also investigates the thermal stability of the GeO_2-passivation for MOS device applications via electrical and material characterization [36]. Germanium (100) pMOSFETs fabricated using the same gate stack show ~1.8× enhancement in effective mobility (μ_{eff}) over control Ge (100) pMOSFETs without GeO_2-passivation and also corroborate the passivating qualities of this RTO-grown GeO_2 interfacial layer. In addition, Ge (111) pMOSFETs with RTO-passivation have also been fabricated that show a high μ_{eff} of ~270 $cm^2V^{-1}s^{-1}$ (at E_{eff}~0.2 MV/cm). For nMOSFET fabrication, the Ge (111) orientation was chosen because of its higher (~1.8×) electron mobility than that of Ge (100) [76]. Germanium (111) nMOSFETs fabricated using the RTO-grown passivation layer show ~2× enhancement in μ_{eff} over control Si (100) nMOSFETs with a high μ_{eff} of ~713 $cm^2V^{-1}s^{-1}$ (at the peak) [39] and thus demonstrate suitability of this RTO passivation approach to achieve Ge CMOS devices with high electron and hole mobility.

1.5.3 Investigation of underperformance in Ge nMOSFETs

In chapter 4, we investigate the RTO-passivated Ge nMOSFETs via temperature-dependent and pulsed I-V characterization [77] to identify the reasons for low μ_{eff} and high I_{OFF} observed in typical Ge nMOSFETs. Temperature-dependent characteristics of the GeO_2/Ge (111) nMOSFETs indicate that despite significant improvement over HF-last devices and a low D_{it} at the mid-gap, the GeO_2-passivated devices still suffer from remote Coulomb scattering. Besides, the ns pulsed I-V characterization suggests significant charge trapping in the gate dielectric that may contribute to the Coulomb-scattering, corroborating the findings of temperature-dependent characterization. In addition, the temperature-dependence of the device characteristics also imply low activation of n-type dopants, and a high density of defects in the S/D junctions formed by ion implantation, which also significantly contribute to the underperformance of these Ge nMOSFETs.

1.5.4 Ge nMOSFETs with n^+/p junctions formed by "Spin-on Dopants"

In chapter 5, we demonstrate a simple approach to form high performance n^+/p junctions in Ge by rapid thermal diffusion of P from "Spin-on Dopants" (SOD) that avoids implantation damage. The junctions formed using this diffusion-based approach show a high I_{ON}/I_{OFF} ratio ($\sim 10^{5\text{-}6}$) and an ideality factor of ~1.03, indicating a low defect density in the junction. The lower defect density in the SOD-doped junctions has been verified by Raman spectroscopy and by the temperature-dependence of off-state leakage. We have also fabricated Ge nMOSFETs with these SOD-doped junctions and a thin RTO-grown GeO_2 passivation layer in the gate stack to integrate the benefits of low D_{it} at the Ge/GeO_2 interface with the low defect density of the SOD-doped junctions.

Furthermore, diffusion-doped Ge (111) nMOSFETs have also been fabricated to investigate the efficacy of this technique on higher mobility (111) orientation.

1.5.5 Ge:C:Mn-on-Si (100), a Si-compatible ferromagnetic material

In chapter 6, we investigate Ge:C:Mn formed by low energy ion implantation on epitaxial Ge:C-on-Si substrates to utilize their Si compatibility and the benefits of 2D confinement in the Ge:C:Mn layer [78-80]. Here we investigate the evolution of magnetic properties of this material as a function of Mn concentration and crystalline structure by varying the Mn implant dose and annealing the sample at different temperatures. The investigation suggests that crystalline structure and Mn concentration of these films play critical role on their magnetic properties.

1.5.6 Workfunction-engineered tunnel barriers for spin injection

In chapter 7, we demonstrate a novel bilayer tunnel barrier for spin-diodes to reduce R_c at the ferromagnetic-metal/semiconductor junctions for novel spin-devices. The proposed tunnel barrier consists of an ultrathin LaO_x/SiO_x stack which forms a dipole and thus reduces the effective Schottky barrier height at the ferromagnetic-metal/semiconductor contact. The Co/n-Si contacts fabricated using these barriers demonstrate significant reduction (~0.3-0.5 eV) in Schottky barrier height and ~4 orders of magnitude decrease in R_c, compared to the control Co/n-Si contacts fabricated using Al_2O_3 tunnel barriers. Such reduction in R_c makes this technique a promising pathway for efficient spin injection into semiconductors.

1.5.7 Summary and future work

Finally in chapter 8 we summarize the dissertation and propose a few approaches to further improve the performance of Ge nMOSFETs and spin-diodes demonstrated in this work.

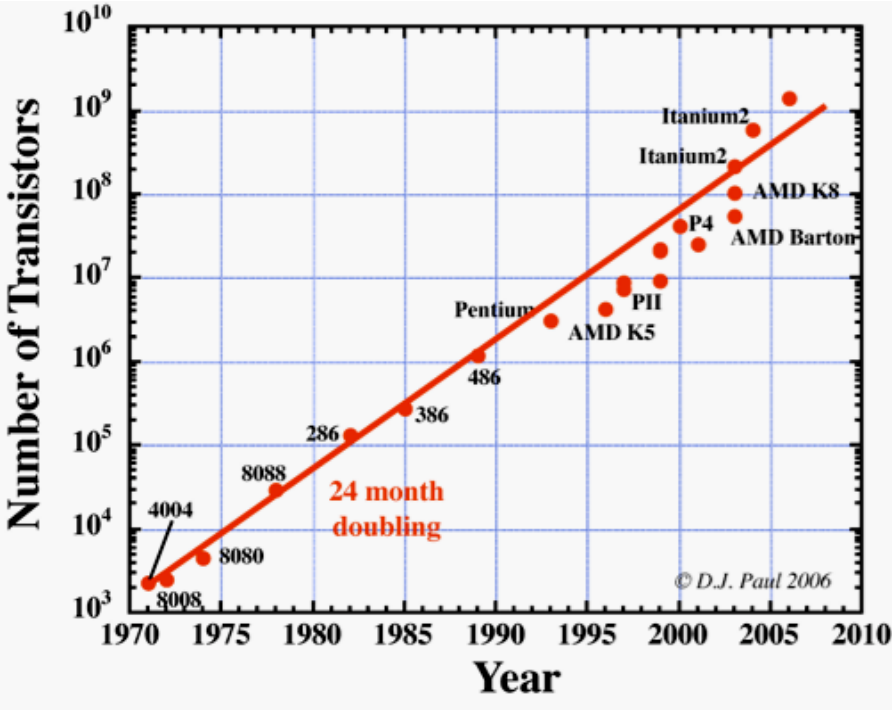


Figure 1.1: Number of transistors in a microprocessors doubles per node (~18-20 months). As predicted by Gordon Moore, this trend dictates the progression of integrated circuits and thus ensures a steady economic return from the CMOS industry.

Source: http://www.sp.phy.cam.ac.uk/~SiGe/Moore's%20Law.html

Device or Circuit Parameter	Scaling Factor
Device dimension *tox, L, W*	1/K
Doping concentration *Na*	K
Voltage *V*	1/K
Current *I*	1/K
Capacitance *εA/t*	1/K
Delay time/circuit *VC/I*	1/K
Power dissipation/circuit *VI*	$1/K^2$
Power density *VI/A*	1

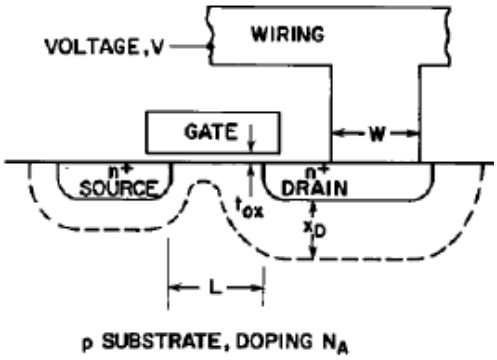


Figure 1.2: Scaling Criteria for circuit performance that improves delay by ~1.4× and shrinks the MOSFETs by ~0.7× times, as proposed by R. H. Dennard [3].

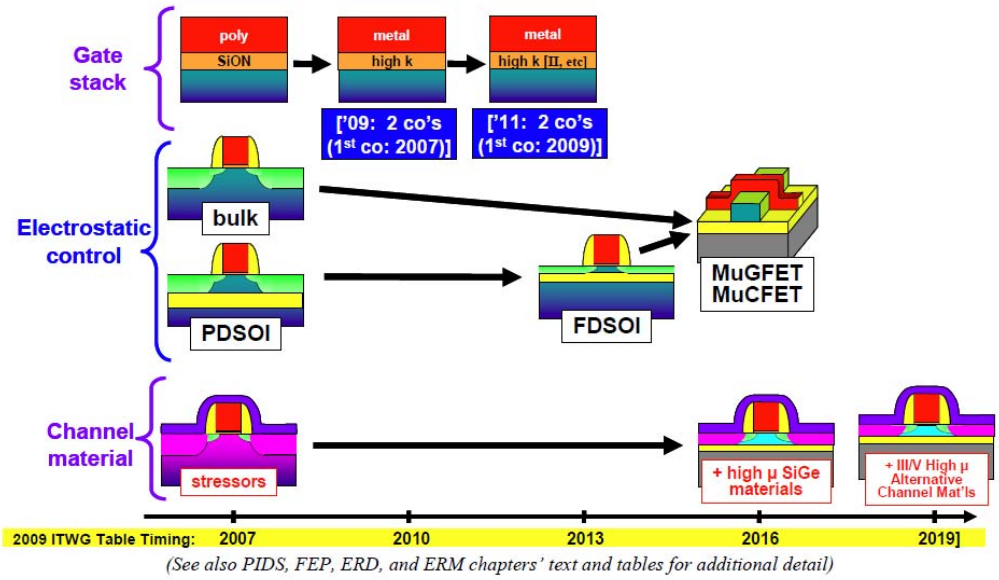


Figure 1.3: Alternative process technologies for equivalent performance scaling [81].

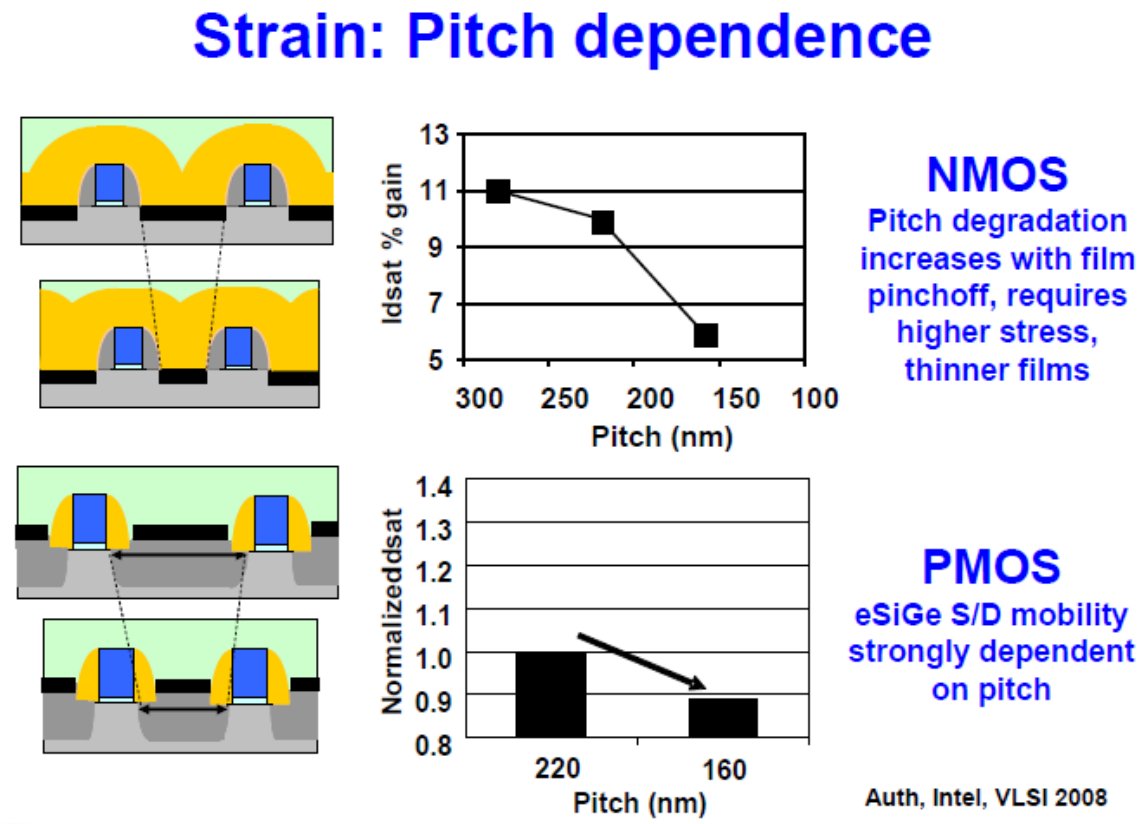


Figure 1.4: Drive current enhancement from strain engineering is getting smaller as the pitch between the devices is getting shorter [14].

Source:http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_SSDM_plenary_slides.pdf

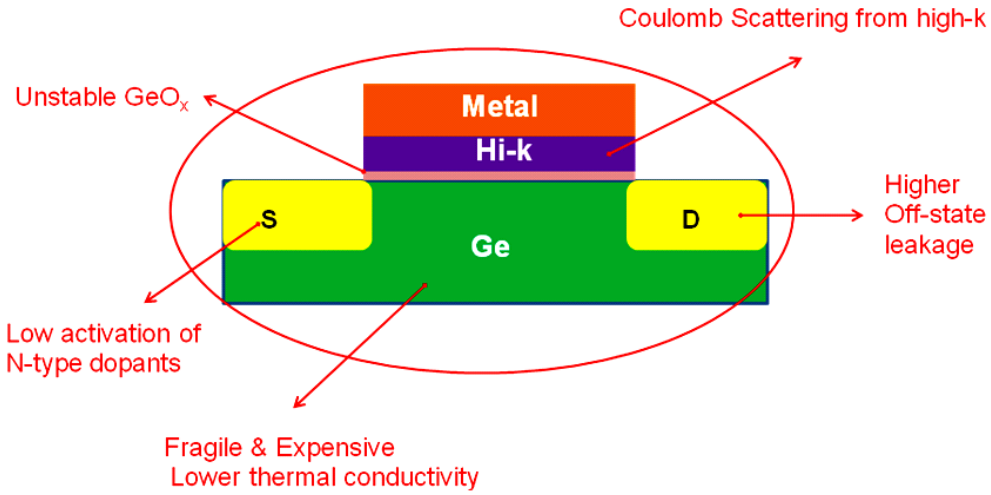


Figure 1.5: Cross-sectional structure of a basic Ge MOSFET, illustrating the major challenges toward high performance CMOS fabrication.

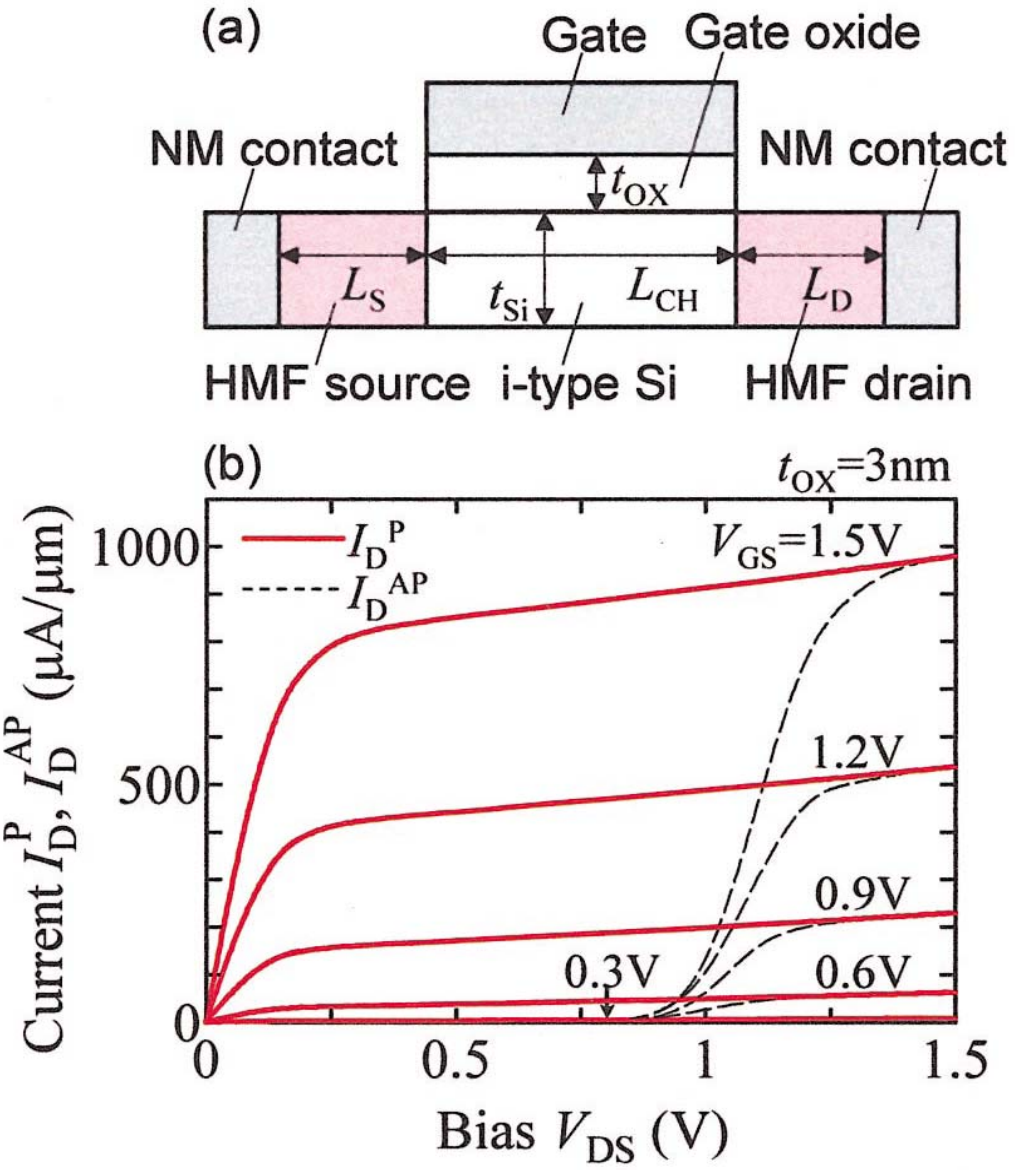


Figure 1.6: (a) Device structure of a conceptual spin MOSFET. (b) Output characteristics of the spin MOSFET. The drain currents I_D^P (solid curves) and I_D^{AP}(dashed curves) in the parallel and antiparallel magnetic configurations, respectively, are plotted as a function of V_{DS} , where V_{GS} is varied from 0.3 to1.5 V [58].

Table 1.1: Material properties of different semiconductor materials [16].

	Ge	Si	GaAs	InSb	InP
Bandgap, E_g (eV)	0.66	1.12	1.42	0.17	1.35
Electron affinity, χ (eV)	4.05	4.0	4.07	4.59	4.38
Hole mobility, μ_h ($cm^2V^{-1}s^{-1}$)	1900	450	400	1250	150
Electron mobility, μ_e ($cm^2V^{-1}s^{-1}$)	3900	1500	8500	80 000	4600
Effective density of states in valence band, N_V (cm^{-3})	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}	7.3×10^{18}	1.1×10^{19}
Effective density of states in conduction band, N_C (cm^{-3})	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}	4.2×10^{16}	5.7×10^{17}
Lattice constant, a (nm)	0.565	0.543	0.565	0.648	0.587
Dielectric constant, k	16.0	11.9	13.1	17.7	12.4
Melting point, T_m (°C)	937	1412	1240	527	1060
Clarke number (%)	6.5×10^{-4}	25.8	Ga: 1×10^{-3} As: 5×10^{-4}	In: 1×10^{-5} Sb: 5×10^{-5}	In: 1×10^{-4} P: 8×10^{-2}

PART I: Ge-BASED CMOS DEVICES

Chapter 2: Effects of Si-Cap Thickness and Temperature on Device Performance of Si/Ge:C/Si pMOSFETs

This chapter discusses the effects of Si cap thickness and temperature on device performance of buried channel Si/Ge:C/Si pMOSFETs. Silicon cap thickness (3 to 9 nm), as well as operating temperature (300K down to 77K), plays a significant role on device performance in terms of drive current, sub-threshold slope, effective hole mobility, and I_{on}-I_{off} ratio. The 7 nm Si capped device demonstrates highest mobility enhancement because of reduced remote Coulomb scattering. In addition, the valence-band offset between the Si-cap/Ge:C interface was quantitatively extracted by fitting the stair-case behavior of split C-V characteristics with self-consistent simulations of one-dimensional Poisson and Schrodinger equations.[ii]

2.1 INTRODUCTION

Germanium has drawn large interest from the semiconductor industry, as a promising material for future CMOS, because of its high intrinsic hole and electron mobility, smaller bandgap and lower processing temperature [16, 19]. However, Ge has its own drawbacks. Bulk Ge wafers are not suitable for current CMOS technology because of their cost, fragility and poor thermal conductivity. Epitaxial Ge grown on Si substrates could be one potential alternative to bulk Ge wafers. However, because of the large (4.2%) lattice mismatch between Si and Ge, it is highly challenging to grow low defect density epitaxial Ge-on-Si [82].

[ii] Part of this chapter is reprinted with permission from [75], © 2010 Institute of Physics.

Another major demerit of Ge is that native GeO_2 is water soluble and unstable, hence cannot be used as a reliable gate dielectric. Moreover, the direct deposition of high-k dielectric on Ge results in high interface state densities (D_{it}) because of interfacial GeO_x ($x<2$) formation, and hence poor device characteristics [16]. Therefore, major developments are going on to integrate an epitaxial Ge channel on a Si substrate [83] and to passivate Ge surface [33] in order to introduce Ge channel-based devices in a CMOS process [84].

In this work, we address both the above mentioned issues by fabricating Si-capped Ge:C devices on epitaxial Ge:C-on-Si substrates. Epitaxial Ge:C layer was chosen over Ge-on-Si because Ge:C shows a low threading dislocation density (TDD ~ $3\times10^5/cm^2$), which is 2-3 orders of magnitude lower than that of epitaxial Ge grown directly on Si substrates. Introduction of trace amounts of carbon (C) (<0.5 in %) into the epitaxial layer facilitates two-dimensional (2-D) growth of Ge:C directly on Si. Because of the low solid solubility of C in Ge, C tends to segregate towards the interface of Ge:C/Si substrate and thus limits the defects near the bottom interface. As a result, the upper portion of Ge:C layer has a much lower defect density than that of pure Ge grown directly on Si (100) [73, 74]. On the other hand, the in situ Si capping of the Ge:C layer prevents GeO_x formation and passivates the Ge:C surface. Moreover, the introduction of a thin Si cap creates a quantum well for holes in the Si/Ge:C/Si structure [28]. Therefore, the Si cap enhances the pMOSFET properties by two means: it passivates the Ge surface and reduces remote Coulomb and surface roughness scattering from the high-k interface, because of the quantum-well structure.

We fabricated Si/Ge:C/Si pMOSFETs to combine the benefits of low defect density of Ge:C film and the passivating qualities of Si cap. In order to investigate the effects of Si cap thickness (3 to 9 nm) on these devices, we carried out a temperature-dependent electrical characterization, along with device

simulations. Drive current, off-state leakage, sub-threshold slope, effective hole mobility and I_{on}-I_{off} (on-state drive current vs. off-state current) ratio depends strongly on Si cap thickness and operating temperature. Split capacitance-voltage (C-V) characteristics of the devices exhibited a stair-case behavior, which was used to determine the gate bias at which a second sub-band, confined primarily in the lower mobility Si cap layer, becomes occupied. Finally, one-dimensional (1-D) Poisson and Schrodinger equation was solved self-consistently to fit the experimental split C-V data in order to extract the valence-band (VB) offset and band alignment between the Si-cap/Ge:C interfaces[85]. The author acknowledges collaboration from En-shao Liu for performing the low-T measurements and the device simulations used in this work to extract the VB offset. The characterization performed provides us with insights about how to design the optimal Si cap thickness for epitaxial Ge-based devices.

2.2 MATERIAL GROWTH AND DEVICE FABRICATION

The MOSFETs were fabricated on epitaxial Ge:C layer (~ 15 nm) grown on lightly doped (1-10 Ω·cm) n-type Si (100) substrate. Epitaxial Ge:C film was grown in a custom-built cold-wall ultra high vacuum chemical vapor deposition (UHV-CVD) system. Disilane (Si_2H_6), methyl-germane (CH_3GeH_3) and germane (GeH_4) gases were used as Si, C and Ge precursors, respectively. Before the epi growth, the substrates were cleaned in a piranha solution followed by a 40:1 de-ionized H_2O:HF dip for 40 s. The base pressure of the UHV-CVD process chamber was ~8×10^{-10} Torr. The Ge:C layer was grown at 420^{o}C at a pressure of 5 mTorr. The temperature was then raised to ~515 ^{o}C to grow the thin Si cap layer. As-grown Ge:C and Si cap thicknesses were measured by ellipsometry and confirmed by X-ray reflectivity (XRR) measurements. Atomic force microscopy

(AFM) and diffraction (XRD) studies were performed to verify the quality of the grown films.

For device fabrication, the epi film was cleaned by 20 minute sonication in acetone followed by isopropanol and DI water rinse. After a brief HF etch, the samples were loaded into the atomic layer deposition (ALD) chamber and ~6 nm HfO_2 was deposited. Post-deposition anneal (PDA) was performed at 500 ^oC for 5 min in N_2 ambient. After PDA, ~200 nm TaN was sputter deposited as a gate metal. Optical lithography and reactive ion etching (RIE) were performed to define the ring-FET. The channel length (L) ranges from 5 to 75 μm, and the gate width (W) ranges from 500 to 1000 μm. As the devices were long channel, no channel implant has been employed. However, a low background doping of $<5\times10^{15}$ cm^{-3} is expected in the epitaxial film. Ion Implantation of BF_2^+ was performed at a dose of 5×10^{15} cm^{-2} and energy of 25 KeV to form the Source/Drain region. The samples were subsequently annealed during a low-temperature oxide (LTO) deposition step for 2 hr at 530 ^oC. As a result, a doping density of $\sim10^{20}$ cm^{-3} is expected in the p^+ region. Aluminum was sputtered to form front and back contacts. Sintering was performed for 30 min, at 450 ^oC in a forming gas ambient.

2.3 RESULTS AND DISCUSSIONS

2.3.1 Material Characterization

The quality of the grown epitaxial films was verified by XRD rocking curves and AFM scans. The improved quality of the grown film is evident from the comparison of the AFM images of Ge on Si and Ge:C on Si films. Three-dimensional (3-D) images of AFM surface scans, performed on 5×5 μm^2 area, are presented in Figure 2.1. The Ge film shows a high root mean square (RMS)

roughness (~1.9 nm) with severe islanding, whereas the Ge:C film shows a smooth surface with a low RMS roughness of ~0.292 nm. The Si-capped (3, 7 and 9 nm) Ge:C films used for device fabrication demonstrated similar low RMS roughness values (0.29- 0.4 nm). Therefore, compared to conventional epi-Ge interface, a smoother epi-Ge:C interface is expected in the fabricated devices. The quality of the grown epitaxial films was further evident from the XRD rocking curves. Figure 2.2(a) shows the XRD rocking curve scanned on (004) hkl plane of a ~15 nm Ge:C on Si (100) film. The Ge:C (004) peak occurs at ~32.95^{o} and the relative position of this peak to the Si (004) substrate peak confirms formation of partially relaxed Ge:C film of (100) orientation with nominal compressive strain. Again, the full width half maximum (FWHM) of the epitaxial Ge:C peak is ~0.23^{o}. Such a low FWHM peak of the thin (~15 nm) epitaxial layer denotes the good crystalline quality of this epitaxial film. Finally, secondary ion mass spectroscopy (SIMS) profile (shown in Figure 2.2(b)) was used to confirm C incorporation in the grown film. Figure 2.2(b) also shows segregation of C atoms near the interface of Ge:C/Si substrate. Presumably, the segregated C atoms near the substrate cause significant strain relaxation [86]. Besides, as the channel region has very low C concentration, the effect of alloy scattering is expected to be less pronounced in the Ge:C devices.

2.3.2 Design of Experiment

Table 2.1 presents the design of experiments carried out in this work. The devices are identified by as-grown Si cap thickness. However, top ~1 nm of the Si cap may have been consumed during surface cleaning prior to dielectric deposition and during subsequent annealing by SiO_x layer formation. 2.3 (a) presents the schematic diagram of the gate stack in a buried-channel Ge:C

pMOSFET device. Figure 2.3 (b) shows the band diagram of the Si/Ge:C/Si structure presented in Figure 2.3 (a). The band diagram demonstrates the presence of a quantum well for holes in the high mobility Ge:C layer. As a result, in addition to passivating the Ge:C surface, Si cap also creates a buried channel for holes in the high mobility Ge:C layer.

2.3.4 Extraction of Valence-band Offset in Si/Ge:C/Si Devices

The split C-V (C_{gc}-V_G) data of these MOSFETs were fitted to a theoretical model to find out the approximate valence band offset between Si-cap and Ge:C (ΔE_v) in the fabricated devices. The simulations have been performed in collaboration with E.S. Liu and the details are described in [85]. Split C-V measurements performed at 77K has been used to minimize the effects of thermionic emission over the hole barrier. Figure 2.4 (a) shows the split C-V characteristics (measured at 77K) of the 3 devices that have been used for this ΔE_v extraction. The stair-case behavior of the split C-V characteristics corresponds to the ΔE_v between the Si cap and Ge:C channel. The simulator developed in [87, 88] was used to solve the 1-D Poisson and Schrödinger equations self-consistently to match the stair-case behavior of the split C-V curves. The effective oxide thickness (EOT), Si cap thickness, Ge:C thickness, and ΔE_v were iteratively adjusted to match the experimental C_{gc}-V_G characteristics. The simulation results for 3, 7 and 9 nm Si cap devices are shown in Figure 2.4 (b), (c) and (d) respectively. Although experimental data and theoretical simulation did not perfectly overlap, the simulations successfully reproduced the Si cap thickness and the signature of C_{gc} data, namely the onset and ending of plateaus and the magnitude of C_{ox}. A ΔE_v of ~660 meV was determined from 3 and 7 nm Si-cap devices. The extracted ΔE_v of ~660 meV is in close agreement with theoretical and experimental estimations performed by

different groups [28, 89][iii]. However, the extracted ΔE_v for the 9 nm Si cap device is ~1060 meV, much larger than expected. The 9 nm Si cap has a high defect density and increased interface state density which causes a stretch-out in the voltage-axis of the C_{gc}-V_G plot. We speculate that this stretch-out in V-axis results in the over-estimation of ΔE_v.

In general, the presence of a large ΔE_v (~660 meV) makes Si cap a promising choice for high-performance buried channel Ge pMOSFET devices. However, as shown in the insets of Figure 2.4 (b), (c) and (d) conduction band (CB) of the Si cap aligns slightly below than that of the Ge:C CB and results in type-II band alignment. Therefore, a quantum well for electrons cannot be achieved in high mobility Ge and this phenomenon makes Si-cap unsuitable for buried channel Ge-based nMOSFETs.

2.3.5 Effects of Si-cap Thickness on Transfer Characteristics

Next, we address the role of the buried channel structure on the pMOSFET electrical characteristics, from room temperature down to 77K. Figure 2.5 presents the saturation drain current vs. gate voltage (I_D-V_G) characteristics (at V_D=-1 V) at 300K as a function of different Si cap thickness. As shown in Figure 2.5, the 3 nm Si cap device shows the lowest I_{off} (at $|V_G-V_T| < 0$V). As the Si cap thickness is increased from 3 nm to 7 nm and 9 nm, I_{off} goes up by ~2× and two orders of magnitude, respectively. The 3 nm Si cap offers more gate control than the other two devices and hence lowest off-state leakage. On the other hand, the 3 nm Si cap device has the highest I_{on} ((measured at $|V_G-V_T| = 2$V)), whereas, the thickest Si cap (9 nm) has the poorest I_{on}. Among the devices, the 9 nm Si cap device has the poorest I_{on}-I_{off} ratio and shows extremely high sub-threshold slope.

[iii] These studies were done for strained-Ge/relaxed-Si interfaces. Theoretical and experimental estimations of valence band offset at strained-Si/relaxed Ge and relaxed-Si/relaxed-Ge interfaces performed by different groups are listed in Appendix A. In practice, in our devices we have a relaxed Si cap on relaxed Ge:C as we have grown beyond critical thickness.

In the case of 9 nm Si cap, channel is formed mostly in the highly defective and rough Si cap, which has a lower mobility than the underlying Ge:C layer. The higher off-state leakage in the thicker (7 and 9 nm) Si-capped devices may be explained by weaker gate control and hence parallel conduction through the higher defect density Si caps. Therefore, a 3 nm Si cap appears to be more optimal than 7 and 9 nm Si caps in terms of higher drive current, lower sub-threshold swing (S) and lower off-state leakage. However, compared to the 7-nm and 9-nm Si cap device, the thinnest (~3 nm) Si cap device showed roughly an order of magnitude increase in gate leakage current density (~$3X10^{-5}$ A/cm^2 at V_G=1V), presumably due to Ge out-diffusion into the high-k dielectric. However, even for the 3 nm Si cap device gate leakage current is a negligible (<0.1%) component of the off-state leakage current.

2.3.7 Extraction of Off-state leakage mechanism from Temperature-dependent Transfer Characteristics

Figure 2.6 presents the temperature-dependent I_D-V_G characteristics measured at V_D= -1 V, for the three different cap thickness. The key data of Figure 2.6 are also presented in Table 2.2, where I_{on} values are measured at $|V_G - V_T|$ = 2 V and I_{off} values are measured as the minimum current of the I_D-V_G traces. As the temperature is reduced from 300K to 77K, I_{off} decreases by ~2-3 orders of magnitude. In order to further investigate the effects of Si cap thickness on I_{off}, Arrhenius plots of I_{off} are presented in Figure 2.7 for (a) linear region (V_D =-50 mV) and (b) saturation region (V_D =-1V). As shown in Figure 2.7 (a), activation energies of the devices decrease with increasing Si cap thickness. The 3 nm Si cap device shows the strongest temperature dependence with an activation energy (E_A) of ~0.32 eV, which is very close to the half of the Ge bandgap (E_G ~0.66 eV). Therefore, we speculate that Shockley-Read-Hall (SRH) generation is the dominant junction leakage mechanism in this device. However, temperature

dependence of I_{off} becomes weaker as Si cap thickness increases from 3 nm to 7 nm (E_A ~0.23 eV) and 9 nm (E_A ~0.1 eV). Such low activation energies are typically attributed to trap-assisted-tunneling (TAT) or band-to-band-tunneling (BTBT) [38, 90]. Presumably defect density in the Si cap region increases with increasing Si cap thickness. As a result, thicker Si cap devices are more prone to TAT and hence show weaker temperature dependence. Again, compared to low drain bias case (V_D =-50 mV), a weaker temperature dependence was observed at higher drain bias (V_D =-1V) as shown in Figure 2.7(b). The stronger temperature dependence at low reverse bias indicates dominance of SRH leakage and TAT. On the other hand, weaker temperature dependence at higher bias indicates increased contribution from BTBT. Interestingly, temperature dependence of I_{off} of the 9 nm Si cap device did not change much with drain bias. Apparently, temperature dependent junction leakage mechanisms are less dominant here and highly defective Si-cap/Ge:C interface acts as a leakage path in the 9 nm Si cap device. On a separate note, drain field dependence of I_{off} in the 3 and 7 nm devices (not shown here) reduced at higher temperatures (near 300K). Similar decrease in field enhancement factor of leakage current (at higher temperatures) in Ge p^+-n junctions has also been observed by the IMEC group [91]. As junction leakage is the major component of I_{off} in our 3 and 7 nm devices, I_{off} is expected to be reduced significantly by adopting junction optimization schemes. Among such schemes utilization of optimized channel/halo implants [38, 90] is a promising approach to reduce I_{off} significantly. Besides, reduction of defect density in the Si cap and in the Ge:C layer is expected to reduce junction leakage to some extent. Formation of S/D junction deep in the lower defect density and wider bandgap Si substrate can also be utilized to reduce the junction leakage.

2.3.8 Effects of Temperature on Drive Current

As temperature is decreased from 300K to 77K, I_{on} increases (Figure 2.6) by ~19%, 28% and 13%, respectively, for the 3, 7 and 9 nm Si cap devices. As a result, both the sub-threshold swing and I_{on}-I_{off} ratio improves significantly at reduced temperatures. Among the fabricated devices, the 7 nm Si cap device shows the highest enhancement in drive-current at 77K. These data suggests that the remote Coulomb scattering is less dominant in the 7 nm Si cap device, which results in more drive current enhancement at lower temperatures. Reduced Coulomb scattering in the 7 nm Si cap device is more evident from the effective mobility (μ_{eff}) vs. inversion charge density (N_{INV}) plots presented in Figure 2.8 and peak μ_{eff} (μ_{peak}) vs. temperature plots presented in the inset of Figure 2.9.

2.3.9 Si-cap Thickness Dependence of Effective Mobility

Figure 2.8 further emphasizes the necessity of optimizing Si cap thickness to achieve highest mobility enhancement. The effective mobility (μ_{eff}) of different devices was extracted from linear I_D-V_G (measured at V_D= -50 mV) and split C-V characteristics (Figure 2.4(a)). Figure 2.8 compares μ_{eff} values extracted at 77K as lower temperature reduces the effects of phonon scattering. In general, all the Ge:C devices show hole mobility enhancement (2×-3×) over the control Si device. The 7 nm Si cap device shows the highest μ_{eff} with ~3× enhancement in peak mobility (μ_{peak}) over control Si devices. The thinnest Si cap (3 nm) device shows about 30% lower mobility compared to the 7 nm Si cap device presumably due to increased remote Coulomb scattering from high-k interface. The thickest (9 nm) Si cap device shows the lowest μ_{eff} with lowest μ_{peak}. The lower μ_{eff} is expected in the 9 nm Si cap device, because the second subband, residing in the low mobility Si cap, starts to populate at lower gate bias (as observed in the split C-V characteristics). As a result, the 9 nm Si cap device shows much lower μ_{eff}

than 3 and 7 nm Si cap device, especially at higher inversion charge densities. Moreover, thick (9 nm) Si cap grown on Ge is well over the critical thickness and highly defective, which results in further mobility degradation. Therefore, it is evident that Si cap thickness needs to be optimized in order to achieve highest mobility enhancement in Ge-based pMOSFETs.

2.3.10 Mobility Degradation Mechanisms

The temperature-dependent μ_{eff} vs. N_{INV} curves of the 7 nm Si cap device is shown in Figure 2.9. As a result of reduced phonon scattering, μ_{eff} increases monotonically at lower temperatures. Throughout the temperature range, peak μ_{eff} (μ_{peak}) increases by ~1.5X as temperature decreases from 300K to 77K. However, this small increment in mobility is less than expected. Figure 2.9 inset presents the temperature dependence of μ_{peak} for the 3, 7 and 9 nm Si cap device. The μ_{peak} vs. temperature data are fitted with a power law expression $\mu_{peak}(T) = \mu_0 T^{-\alpha}$. At low temperatures, the reported value of α for holes is ~1 for high quality HfO_2/Si (100) pMOSFETs [92]. For the Ge:C devices investigated in this work, α is ~0.22, ~0.33 and ~0.26 in 3, 7 and 9 nm Si cap thicknesses respectively, indicating a weaker temperature dependence of the hole mobility in our devices. As expected, the 7 nm Si cap device demonstrates the strongest temperature dependence. This observation corroborates our hypothesis that 7 nm Si cap ensures buried channel operation and hence reduces remote Coulomb scattering. The weak temperature dependence of μ_{eff} observed in our devices suggests that the effective mobility of these devices is not limited by phonon scattering but by extrinsic factors (e.g. remote Coulomb scattering from high-k dielectric and surface roughness scattering). Therefore, the hole mobility in Ge:C devices is expected to be enhanced significantly by improving the quality of the deposited high-k oxide.

2.4 SUMMARY

The valence band offset and band-alignment between Si-cap/Ge:C interfaces have been extracted from the fabricated pMOSFETs. The large valence band offset and better high-k interface make Si cap a promising option for passivating Ge-based high mobility pMOSFETs. The device characteristics presented in this paper corroborates the fact that Si cap helps to create a high mobility buried channel Ge pMOSFET with improved performance. However, if the Si cap is too thick, it becomes highly defective and the cap itself acts as a low mobility channel. In summary, this work confirms the necessity to use optimal Si cap layer for high performance buried channel Ge-based pMOSFETs.

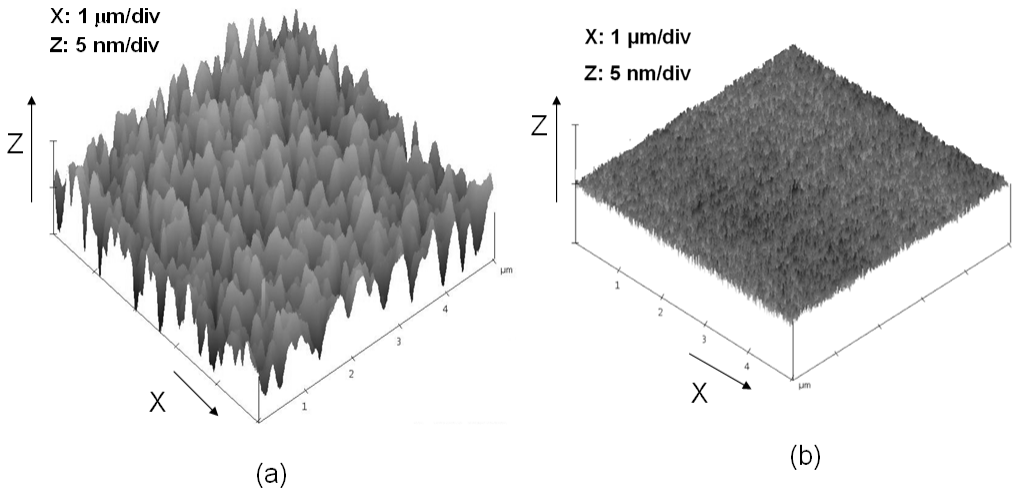


Figure 2.1: AFM images showing 3-D views of the grown films over 5×5 μm^2 area – (a) Ge on Si (100), (b) Ge:C on Si (100). Epitaxial Ge film shows an RMS roughness of ~1.9 nm; whereas Ge:C film shows much lower RMS roughness (~0.292 nm). RMS roughness is improved by ~6× in Ge:C film, presumably due to the strain relaxation at the interface of Ge:C and Si substrate [75].

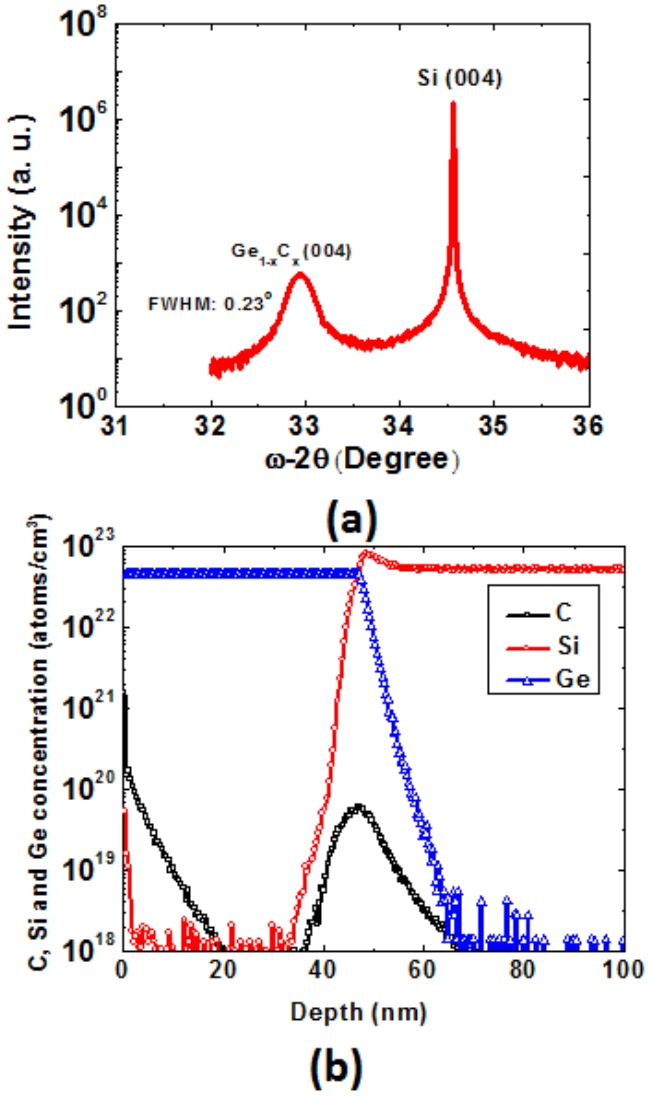


Figure 2.2: (a) XRD rocking curve of 3 nm Si-capped Ge:C (~15 nm) grown directly on Si (100). The relative position of the epitaxial peak to the substrate Si (004) peak confirms formation of partially relaxed epitaxial Ge:C on Si (100). (b) Secondary ion mass spectroscopy (SIMS) profile of a Ge:C (~42 nm) film grown directly on Si (100) substrate. Carbon concentration peaks at the bottom Ge:C/Si substrate interface [75].

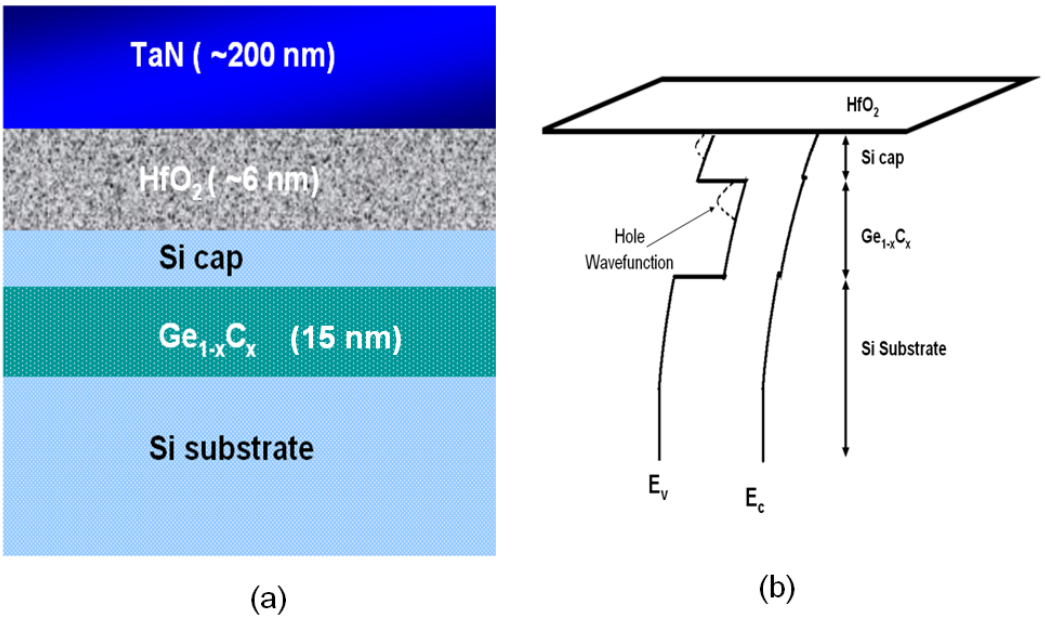


Figure 2.3: (a) Schematic diagram of the gate stack in a buried-channel Ge:C pMOSFET. Si cap thickness was varied (3, 7 and 9 nm). (b) Band diagram (perpendicular to the MOSFET channel direction) of a Si/Ge:C/Si device. Valence band offset creates a quantum well for holes [75].

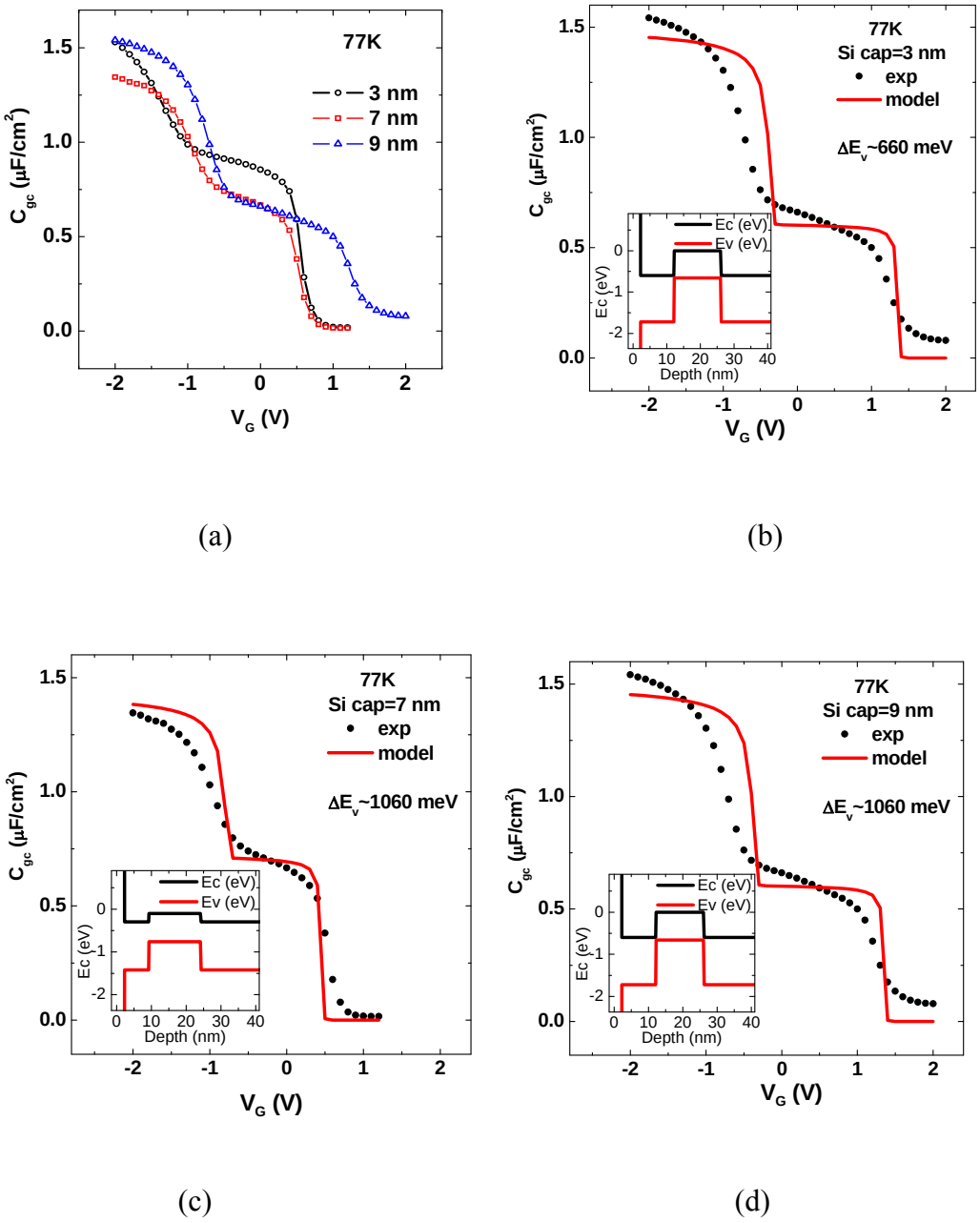


Figure 2.4: Experimental data and theoretical modeling of C_{gc}-V_G characteristics – (a) C_{gc}-V_G characteristics measured at 77K, (b-d) fitting of experimental data with simulation results. The results are shown for different Si cap thickness devices- (b) 3 nm, (c) 7 nm, and (d) 9 nm. Insets of (b), (c) and (d) show the simulated band diagram for the respective devices. Theoretical model successfully reproduce the signature of C_{gc} data, namely the onset and ending of plateaus and the magnitude of C_{ox} [75] [85].

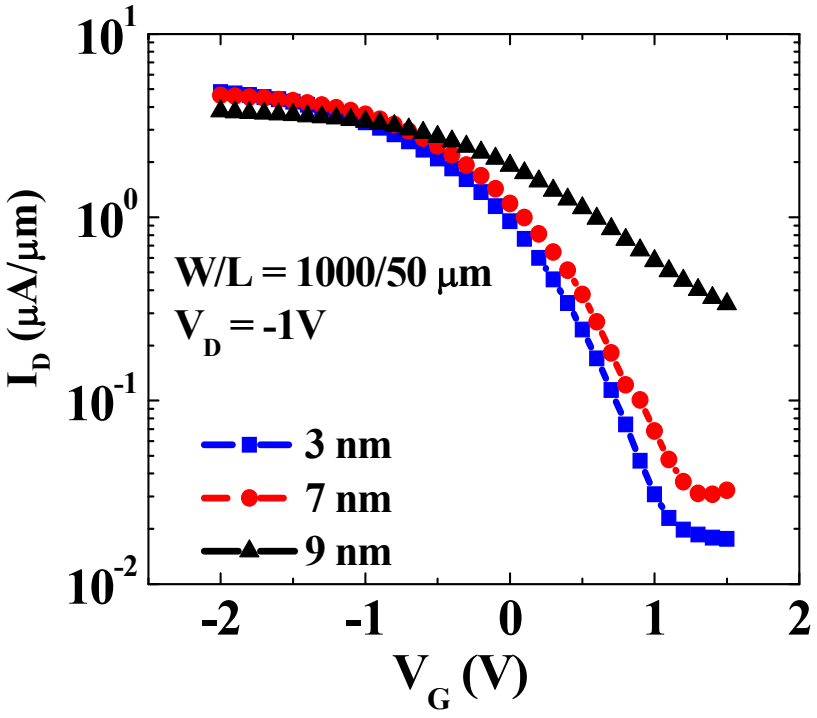
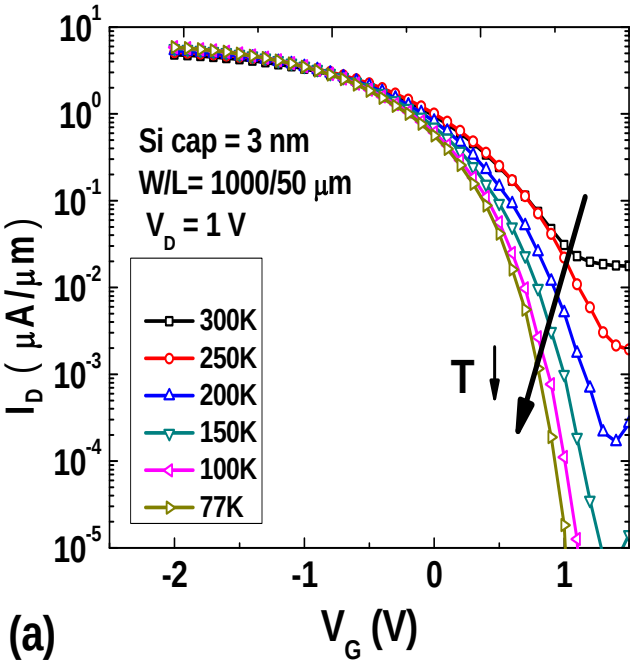
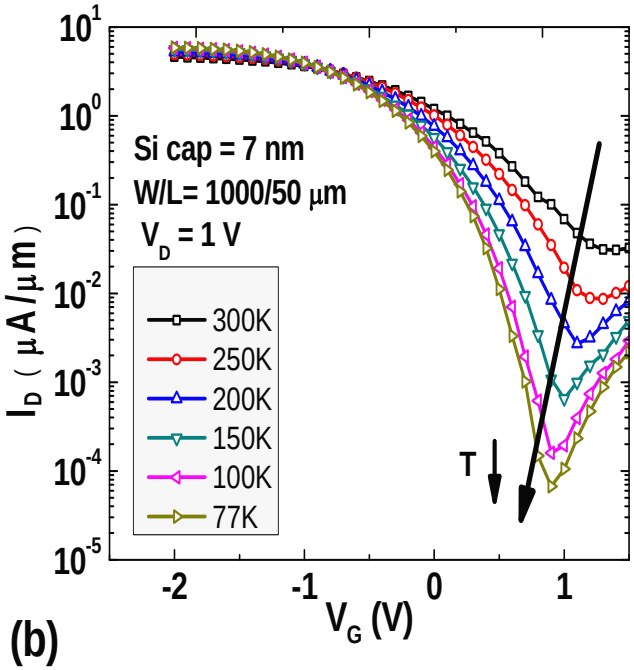


Figure 2.5: Transfer characteristics of the fabricated pMOSFETs (W/L =1000 μm /50μm) at V_D = -1V (measured at 300K). The 3-nm Si cap device demonstrates strongest gate control [75].


Si cap = 3 nm
W/L= 1000/50 μm
V_D = 1 V
300K
250K
200K
150K
100K
77K
T
I_D (μA/μm)
V_G (V)
(a)


Si cap = 7 nm
W/L= 1000/50 μm
V_D = 1 V
300K
250K
200K
150K
100K
77K
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I_D (μA/μm)
V_G (V)
(b)

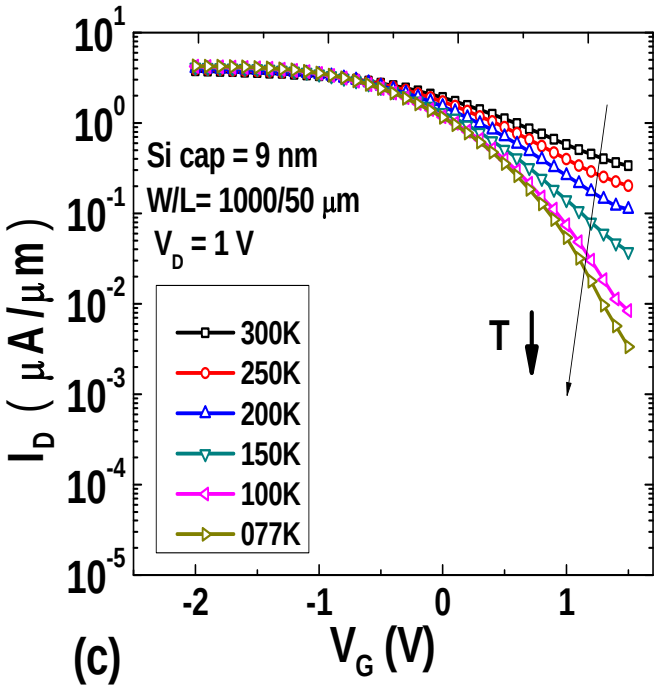

Figure 2.6: Temperature dependence of transfer characteristics in saturation region (V_D = -1V) of varying Si cap thickness devices – (a) 3 nm, (b) 7 nm, (c) 9 nm [75].

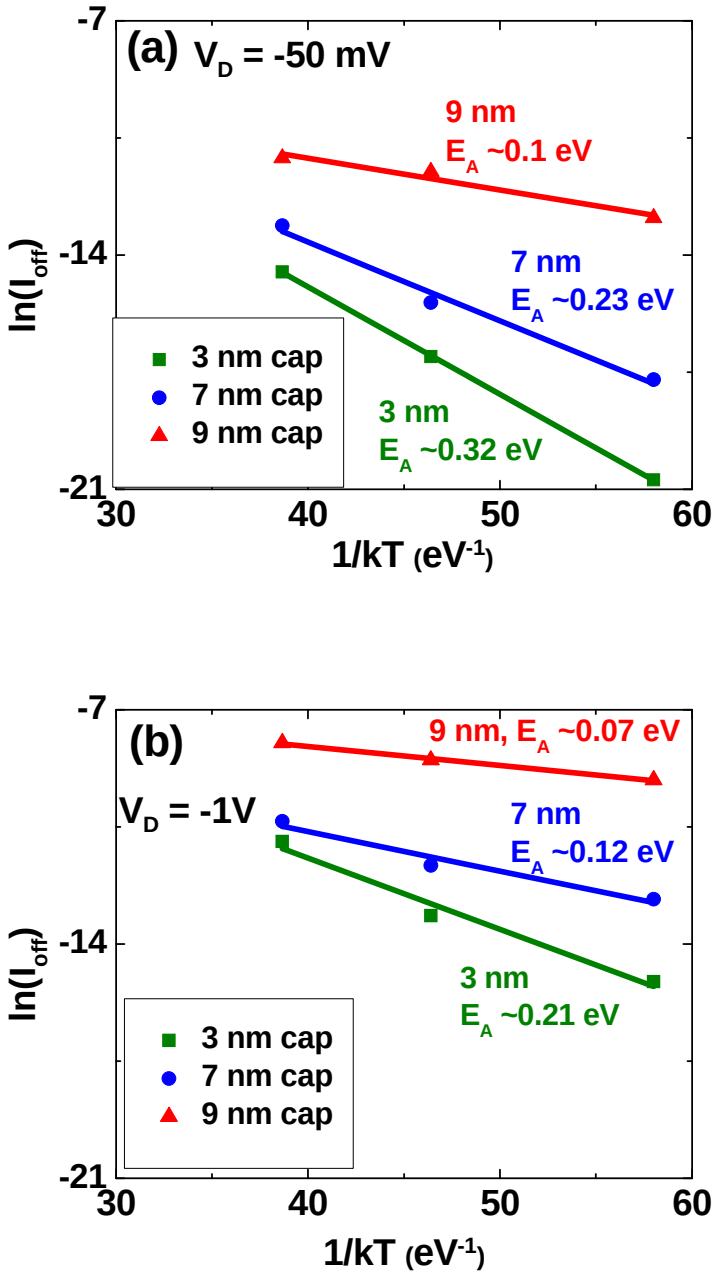

Figure 2.7: Arrhenius plots of I_{off} (measured at V_G=V_{FB}) of the devices with different Si cap thicknesses- (a) V_D=-50 mV and (b) V_D=-1V. Activation energy (E_A) of I_{off} decreases with increasing Si cap thickness and increasing drain bias [75].

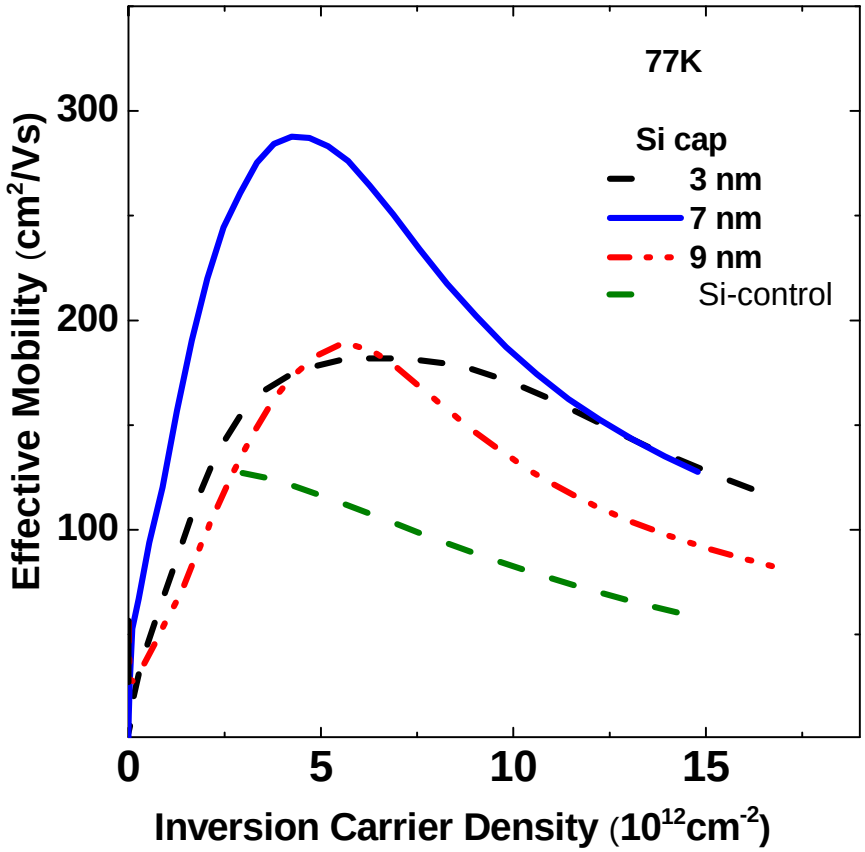

Figure 2.8: Silicon cap thickness dependence of effective mobility (measured at 77K) vs. inversion charge density for the fabricated devices. The 7-nm Si cap device shows highest $\mu_{eff,}$ presumably because of reduced remote Coulomb scattering [75].

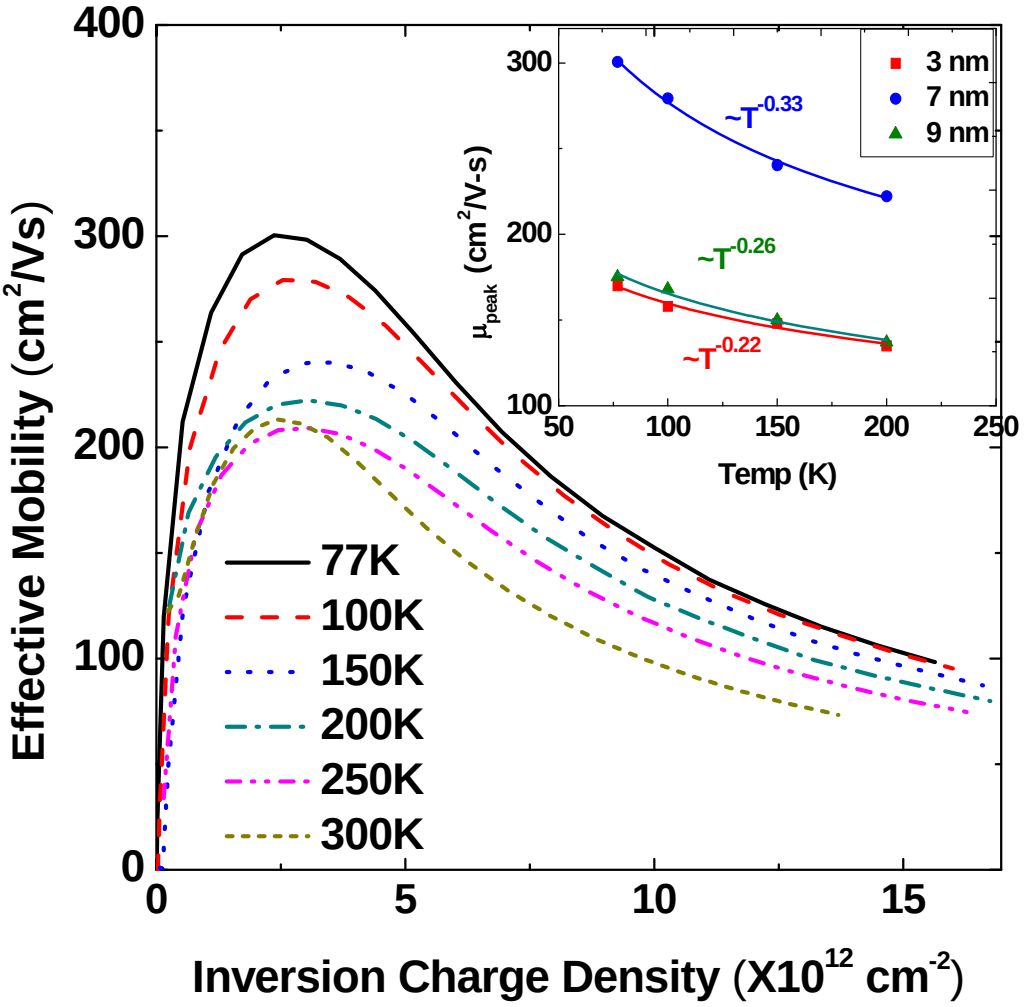

Figure 2.9: Temperature dependence of effective hole mobility vs. inversion charge density curves of 7 nm Si cap device (from 77K to 300K). Inset shows the peak mobility vs. temperature plot of the 3, 7 and 9 nm Si capped devices. The 7 nm Si cap device demonstrates strongest temperature dependence [75].

Table 2.1: Design of Experiment

Sample	**Si cap (nm) (as grown)**	**Ge:C (nm)**
A	3	15
B	7	15
C	9	14

Table 2.2: Summary of I_{on}, I_{off} and I_{on}/I_{off} data (from Figure 2.6)

	300K			**77K**		
Si cap (nm)	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}
3	4.70	1.76×10^{-2}	2.67×10^{2}	5.60	1.3×10^{-6}	4.31×10^{6}
7	4.60	3.1×10^{-2}	1.50×10^{2}	5.87	6.7×10^{-5}	8.76×10^{4}
9	3.77	3.3×10^{-1}	1.13×10^{1}	4.26	3.2×10^{-3}	1.32×10^{3}

Chapter 3: High mobility Ge MOSFETs with GeO_2-Passivation Layer Grown by Rapid Thermal Oxidation

This chapter describes development of a simple route to passivate Ge surface using a thin GeO_2 passivation layer grown by rapid thermal oxidation. In addition, this chapter also investigates the thermal stability of the GeO_2-passivation for MOS device applications. Introduction of a thin (~1 nm) GeO_2 layer to passivate the high-k/Ge interface in $TaN/Al_2O_3/Ge$ MOSCAPs results in a low D_{it} (~9×10^{11} $cm^{-2}eV^{-1}$); whereas, the MOSCAPs without GeO_2 show about an order of magnitude higher D_{it} (~1×10^{13} $cm^{-2}eV^{-1}$). Material and electrical characterization of the MOS devices after various post-metallization anneals show that the highest processing temperature of the GeO_2-passivated devices should be limited to 400ºC to take advantage of the low D_{it} at the GeO_2/Ge interface, as GeO_2 is not stable above 400ºC. As a result of the low D_{it} at the Ge/GeO_2 interface, the GeO_2-passivated pMOSFETs show an enhancement of ~1.8× (at E_{eff} of ~0.25 MV/cm) in effective hole mobility and ~2 orders of magnitude improvement in I_{ON}/I_{OFF} ratio. The GeO_2-passivated nMOSFETs fabricated on higher electron mobility Ge (111) surface, demonstrate a high effective mobility (713 $cm^2V^{-1}s^{-1}$ at the peak) with ~2× enhancement over control Si (100) devices. Moreover, at a drain bias of 1V and at a gate over drive of 1.2V, Ge MOSFETs (L~75 μm) show a drive current of ~1.1 mA/mm, which is ~1.6× higher than that of the control Si devices. In addition, a good subthreshold slope of ~130 mV/decade is achieved in nMOSFETs with the GeO_2 passivation layer[4].

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3.1 INTRODUCTION

As discussed in the previous chapters, despite the attractive qualities of Ge as a channel material for future complementary metal oxide semiconductor (CMOS) devices, there are several challenges towards realization of high performance Ge-based CMOS devices. Among them, the passivation of the Ge/high-k dielectric interface remains a difficult challenge [16, 23]. Although high mobility Ge pMOSFETs have been demonstrated by employing different passivation schemes [25, 29, 75, 93], Ge nMOSFETs fabricated using similar and different schemes resulted in much lower inversion channel mobility than Si nMOSFETs [24, 25, 27, 94], despite higher intrinsic electron mobility in Ge. The major reason for low electron mobility has been recently suggested to be the high interface state density (D_{it}) near the conduction band (CB) edge [31, 32]. However, there are only a few recent passivation schemes using GeO_2-based gate dielectrics (e.g. by ozone oxidation [33] and high pressure oxidation [35]), which showed low D_{it} near the CB edge [33] and relatively high μ_{eff} [40, 95].

In this work, we investigate a novel and simple route to grow GeO_2 by rapid thermal oxidation (RTO), and demonstrate high mobility Ge p- and nMOSFETs using the RTO-grown GeO_2 as an interfacial layer. In order to combine the benefits of higher dielectric constants of high-k oxides and lower D_{it} at the GeO_2/Ge interface, we have integrated a thin (~1 nm) GeO_2 interfacial layer (IL) between Ge and a high-k oxide. Furthermore, RTO-passivation on Ge (111) orientation was also investigated because of its higher (~1.8×) electron mobility [96] and hole mobility [97] than Ge (100).

Towards this goal, TaN/Al_2O_3/GeO_2/Ge MOS capacitors (MOSCAPs) were fabricated and chemical stoichiometry of the interfacial GeO_2 was investigated by X-ray photoelectron spectroscopy (XPS). Improved capacitance-voltage (C-V) characteristics of

the GeO_2-passivated MOSCAPs over the MOSCAPs without GeO_2 demonstrate the benefits of interfacial GeO_2 incorporation. Thermal stability of the GeO_2-passivated devices was investigated via material and electrical characterization of the MOSCAPs after various post-metallization anneals (PMA).

Germanium (100) pMOSFETs fabricated using the same gate stack show ~1.8× enhancement in effective mobility (μ_{eff}) over control Ge (100) pMOSFETs without GeO_2-passivation. The GeO_2-passivated Ge (111) nMOSFETs show ~2× enhancement in μ_{eff} over control Si (100) nMOSFETs [39]. The lower D_{it} and higher mobility observed in the GeO_2-passivated MOS devices demonstrate that an RTO-grown interfacial layer may provide a simple route to passivate Ge and hence, to achieve high mobility in Ge CMOS devices.

The author acknowledges Shagandeep Kaur for her help to perform the XPS measurements.

3.2 DEVICE FABRICATION

Figure 3.1 summarizes the process flow and shows the device structure used in this work for MOS device fabrication. In order to grow the GeO_2 passivation layer, Ge wafers were cleaned by cyclic HF and DI water rinse and then were loaded into a rapid thermal processing system. About 1 nm thick GeO_2 interfacial layer was grown at 400°C for 3 min in an O_2 ambient. After the RTO step, ~7.5 nm thick Al_2O_3 was deposited as the high-k gate dielectric using atomic layer deposition (ALD) technique. After the dielectric deposition, ~200 nm thick TaN was deposited as a metal gate via DC sputtering. The MOSCAPs were defined by optical lithography, followed by reactive ion etching of the TaN metal gate using CF_4 plasma. Control Ge MOSCAPs were fabricated

without any GeO_2 growth. Ring type MOSFETs (channel length, L=5 to 75 μm) were fabricated using the same gate stack.

For pMOSFET fabrication, implantation of BF_2^+ ions (5×10^{15} cm^{-2}) was performed at 25 keV to form the S/D regions, and an activation anneal was performed at 400 °C for 10 min in N_2 ambient, followed by Al deposition as the front and back metal contacts. Forming gas anneal was performed at 400°C for 20 min to improve the S/D contacts. Control Si pMOSFETs and Ge pMOSFETs without GeO_2, were also fabricated, using the same process flow and thermal budget.

For nMOSFET fabrication on Ge (111) orientation, implantation of P^+ ions (1×10^{15} cm^{-2}) was performed at 23 keV to form the S/D regions, and an activation anneal was performed at 400 °C for 10 min in N_2 ambient, followed by Al deposition for front and back metal contacts. Forming gas anneals were performed at 400 °C for 120 min to improve the S/D contacts and to achieve reasonable n-type dopant activation. Control Si (100) nMOSFETs were also fabricated, using the same process flow and thermal budget.

3.3 RESULTS AND DISCUSSION

3.3.1 Stoichiometry of RTO-grown GeO_x

The stoichiometry of the interfacial GeO_2 layer was investigated by measuring the 3d spectra of Ge during monochromatic XPS analysis (Figure 3.2(a)). Three different samples were analyzed: sample A has RTO-grown GeO_2, sample B is HF-last (without GeO_2 growth) and sample C is de-ionized (DI) water-rinsed after the RTO-growth of GeO_2. It may be noted that stoichiometric GeO_2 is water-soluble, and hence we do not expect any oxidation peak in sample C. In sample A (with GeO_2), the separation between the Ge 3d 0^+ peak and oxide peak is ~3.1 eV, which indicates formation of 4^+ oxidation

state rich GeO_2 [98]. On the other hand, the 3d spectra from the HF-last sample do not show any peak corresponding to 4^+ oxidation state. Presumably, the shoulder in the 3d spectra of the HF-last sample indicates presence of native GeO_x (x~1) suboxides, which may have detrimental effects on the gate stack. As expected, no oxidation peak was observed from sample C, which shows the water-solubility of RTO-grown GeO_2 and further corroborates its stoichiometry.

Furthermore, we have investigated the effects of RTO ramp rate on GeO_2 quality by measuring the XPS 3d spectra (inset of Figure 3.2 (b)) from two different GeO_2 samples grown at different ramp rates. The oxide peak from the slower ramp rate (1ºC/s) sample shows a shift of ~0.3 eV towards lower energy as compared to the faster ramp rate (80ºC/s) sample, which suggests an increased presence of lower oxidation states. We hypothesize that the faster ramp rate reduces oxidation of Ge during ramp up and hence reduces sub-oxide formation at lower temperatures. Thus, RTO may offer a benefit over conventional thermal oxidation by reducing formation of lower oxidation states.

3.3.2 C-V characteristics of RTO-passivated MOSCAPs

Figure 3.3 shows the C-V characteristics of the MOSCAPs fabricated in this study on p-Ge (100) substrates (~0.1 Ω-cm). Figures 3.3(a) and (b) compare the characteristics of the as-fabricated devices, where the GeO_2-passivated MOSCAPs show less frequency dispersion than the HF-last MOSCAPs. The advantage of the GeO_2-passivation layer is even more evident from the C-V characteristics of the optimized devices after a post-metallization anneal (PMA) performed at 400ºC for 5 min, as shown in Figures 3.3(c) and 3.3(d). After this PMA in N_2-ambient, the optimized GeO_2-passivated MOSCAPs show negligible frequency dispersion (10-1000 kHz), compared to the HF-last MOSCAPs. Moreover, the HF-last MOSCAPs show a kink in the C-V curve and

inversion-like C-V behavior at high-frequencies (10-1000 kHz), which indicates a high D_{it}. On the other hand, the MOSCAPs with GeO_2 show a lower mid-gap D_{it} (extracted by quasi-static C-V method) of ~9×10^{11} $cm^{-2}eV^{-1}$, which is lower than that (~7-8×10^{12} $cm^{-2}eV^{-1}$) of the HF-last MOSCAPs by about an order of magnitude.

3.3.3 Optimization of RTO-growth temperature

With a view to fabricating higher electron mobility Ge (111) MOSFETs, we have optimized the RTO conditions by investigating GeO_2-passivated MOSCAPs on lightly p-type (~10-20 Ω-cm) Ge (111) substrates. It appears, among other conditions, RTO temperature plays the most critical role on the quality of the grown passivation layer. For instance, Figures 3.4 (a) and (b) show the bi-directional C-V characteristics of the Ge (111) MOSCAPs with the GeO_x-passivation layer grown for 3 min at 400°C and at temperatures higher than 400ºC. Among the fabricated MOSCAPs, the devices with GeO_x layer grown at 400ºC show the minimum hysteresis, indicating the lowest D_{it}. Besides, the MOSCAPs fabricated with GeO_x layer grown at 500ºC and higher show significantly higher equivalent oxide thicknesses (EOT), presumably due to the thicker growth of GeO_x and therefore, are not interesting from a device scaling perspective.

The MOSCAPs fabricated with the GeO_x layer grown at 450ºC, show a large hysteresis, which is possibly due to the sub-stoichiometric growth of GeO_x ($x<2$) at 450ºC. The sub-stoichiometric growth at about 450ºC is expected, as GeO_2 start to react with Ge and form volatile GeO following equation (3.1) at ~430-450ºC.

$$GeO_2 + 2Ge \xrightarrow{430°C} 2GeO \qquad (3.1)$$

Formation of lower oxidation states at 450ºC is also evident from the XPS 3d spectra of the GeO_x passivation layer grown at 400ºC and 450ºC, as shown in Figures 3.4 (c) and (d). The position of the peak from the GeO_x grown at 400ºC, confirm growth of

GeO_2 at 400ºC with more 4^+ oxidation states. On the other hand, the peak from the GeO_x layer grown at 450ºC is weaker and also shifts toward the Ge 2^+ state by about ~0.26eV, indicating stronger presence of volatile and unstable GeO, which results in a high D_{it} at the high-k/Ge interface.

3.3.4 Thermal-stability of GeO_2-passivated devices

The thermal stability of the GeO_2-passivated Ge (111) MOSCAPs was investigated through various PMA treatments. It appears that the passivating qualities of the GeO_2 layer is retained after long PMA performed at 400ºC for 30 min in N_2 ambient. However, the benefits of GeO_2-based passivation are lost even after a PMA performed at 450ºC for only 5 min, which is presumably due to the desorption of GeO_2 at ~450ºC as governed by equation (3.1). Figures 3.5(a) and (b) show the XPS 3d spectra from the Al_2O_3 (~3.5 nm)/GeO_2 (~1 nm)/Ge (111) stack after anneals at 400ºC and 450ºC for 5 min in N_2 ambient. The oxide peak observed from the sample annealed at 450ºC is weaker and shows a shift toward lower energy than that from the sample annealed at 400ºC, which confirms formation of GeO during PMA performed at 450ºC or higher. As a result of such decomposition of the GeO_2 layer, the D_{it} at the high-k/Ge interface increases significantly. The increased D_{it} of the MOSCAPs annealed at 450ºC results in a larger hysteresis (>300 mV), compared to that (<100 mV) of their counterparts annealed at 400ºC, as shown in Figure 3.5(c). Furthermore, formation of volatile GeO at higher temperatures also degrades the gate stack reliability, presumably by creating traps in the high-k dielectric. This degradation in the high-k reliability is evident from Figure 3.5(d), which shows an increase of ~2 orders of magnitude in the leakage current density (at V_G =-1.5V, in accumulation) of the Ge (111) MOSCAPs annealed at 500°C for 5 min.

To summarize the thermal stability study performed in this work, the highest processing temperature of the GeO_2-passivated MOS devices needs to be limited to 400°C or lower in order to maintain the benefits of low D_{it} at the Ge/high-k interface. This temperature of 400°C is high enough to achieve good activation of p-type dopants in Ge [99], however, it is not high enough to achieve a reasonable activation of n-type dopants [100].

3.3.5 RTO-passivated Ge pMOSFETs

In order to investigate the effects of the RTO-grown GeO_2 passivation in a MOSFET structure, we have fabricated gate-first $TaN/Al_2O_3/GeO_2/Ge$ pMOSFETs on n-Ge (100) substrates (~0.005-0.02 Ω-cm). Control devices without the RTO-passivation were also fabricated on the same substrates. The GeO_2-passivated Ge (100) pMOSFETs clearly outperform the control Ge (100) devices and hence demonstrate the benefits of GeO_2 passivation in a MOSFET structure. Figure 3.6 (a) shows the linear I_S-V_G characteristics (at V_D = 50 mV) of long channel (L~75 μm) pMOSFETs with and without GeO_2 passivation, respectively. The GeO_2/Ge (100) pMOSFETs demonstrate a good I_{ON}/I_{OFF} ratio of ~10^5, a low subthreshold slope (SS) of ~119 mV/decade, and a threshold voltage (V_T) of ~ -0.6 V. On the other hand, the devices without GeO_2 show a low I_{ON}/I_{OFF} ratio of ~10^3, a high SS of ~223 mV/decade, and a threshold voltage (V_T) of ~0.4 V. The low SS of ~119 mV/decade, indicates a relatively low D_{it} (~$2\text{-}3\times10^{12}$ $cm^{-2}eV^{-1}$) at the GeO_2/Ge interface even after MOSFET fabrication. Furthermore, compared to the control devices, the GeO_2-passivated devices (L ~75 μm) show ~1.2× enhancement in drive current with a drive current of ~0.6 μA/μm in the saturation region (V_D= 1V) at a gate overdrive of ~1 V (Figure 3.6 (a)).

Figure 3.7 shows the μ_{eff} vs. effective field (E_{eff}) plots of the same devices, where μ_{eff} is extracted from their respective I_S-V_G (at V_D= 50 mV) and split C-V characteristics. The GeO_2-passivated devices show ~1.8× enhancement (at E_{eff}=0.25 MV/cm) in μ_{eff} over the control devices, and also surpasses the universal Si mobility. It may also be noted that the mobility data shown are not corrected for the S/D series resistance (R_S). Therefore, performance of these devices is limited to some extent by their R_S and hence is expected to be further improved by reducing the S/D R_S by optimizing the dopant activation and metal-germanidation processes.

3.3.6 RTO-passivated Ge (111) pMOSFETs

In order to investigate the performance of Ge pMOSFETs on higher electron mobility (111) orientation, GeO_2-passivated pMOSFETs were also fabricated on n-Ge (111) substrates (~5-40 Ω-cm). The μ_{eff} vs. E_{eff} data of these Ge (111) pMOSFETs are shown in Figure 3.8 that demonstrate a high μ_{eff} of ~270 $cm^2V^{-1}s^{-1}$ for holes, with ~2.3× enhancement over universal Si mobility and ~1.5× enhancement in μ_{eff} over the devices on heavily-doped Ge (100) substrates (~0.005-0.02 Ω-cm). The higher hole mobility observed in the GeO_2/Ge (111) devices may be attributed in part to the higher mobility on (111) surface [97] and the lower impurity scattering due to the lower density of n-type dopants in the starting substrate [101] . Nevertheless, the high hole mobility observed in these (111) devices envisage the promise of this RTO-passivation technique to fabricate high mobility Ge-based CMOS on Ge (111), as this orientation is expected to have the highest electron mobility in Ge.

3.3.7 RTO-passivated Ge (111) nMOSFETs

In order to investigate the effects of the RTO-grown GeO_2 passivation on nMOSFET performance and to take the advantage of higher electron mobility on Ge

(111) orientation, we have fabricated gate-first TaN/Al_2O_3/GeO_2/Ge (111) nMOSFETs on p-Ge (111) substrates (~10-20 Ω-cm). Control Si devices were also fabricated on the p-Si (100) substrates (~1-10 Ω-cm). The GeO_2-passivated Ge (111) nMOSFETs clearly outperform the control Si (100) nMOSFETs and hence demonstrate the benefits of GeO_2 passivation in a MOSFET structure. Figure 3.9 shows the linear I_D-V_G characteristics (at V_D = 50 mV) of long channel (L~75 μm) Ge (111) and Si (100) nMOSFETs. The GeO_2/Ge (111) nMOSFET demonstrates a good I_{ON}/I_{OFF} ratio of $>10^3$,a low subthreshold slope (SS) of ~130 mV/decade, and a threshold voltage (V_T) of ~0.25 V. In general, compared to the drain current, the source current of Ge devices is less affected by the S/D junction leakage. As a result, the I_S-V_G plot (also shown in Figure 3.9) of the same GeO_2/Ge (111) device shows a higher I_{ON}/I_{OFF} ratio of $\sim10^4$ and a lower SS of ~113 mV/decade, which indicates a relatively low D_{it} ($\sim3\times10^{12}$ $cm^{-2}eV^{-1}$) at the GeO_2/Ge interface. Furthermore, the transconductance (g_m) (inset (a) of Figure 3.9) of the GeO_2/Ge (111) MOSFET shows a ~2.2× enhancement over the Si MOSFET in the linear region. Inset (b) of Figure 3.9 shows the output characteristics of the Ge (111) and control Si (100) nMOSFETs (L= 75 μm). In the saturation region, and at a gate overdrive of ~1.2 V, the Ge device shows a drive current of ~1.1 mA/mm, which is ~1.6× higher than that of the control Si device.

Figure 3.10 (a) shows the μ_{eff} vs. effective field (E_{eff}) plots of the same devices, where μ_{eff} is extracted from their respective I_D-V_G (at V_D= 50 mV) and split C-V characteristics. The Ge nMOSFET shows ~2× enhancement over the Si control device with a high peak μ_{eff} of ~713 $cm^2V^{-1}s^{-1}$, which is comparable to the universal Si mobility at low effective fields. The peak μ_{eff} occurs at an inversion charge density (N_{INV}) of $\sim2.1\times10^{11}$ cm^{-2}, measured at a gate overdrive of ~150 mV. The mobility data from three different devices have been compared, all of which exhibited comparable peak μ_{eff} of

~700 $cm^2V^{-1}s^{-1}$ at N_{INV} of ~2-3.5×10^{11} cm^{-2}. This observation is in agreement with [102], where the peak μ_{eff} is observed at similarly low N_{INV} of ~1-2×10^{11} cm^{-2} in Ge nMOSFETs fabricated on lightly doped substrates. The mechanism that leads to a peak μ_{eff} at such low N_{INV} in lightly doped Ge nMOSFETs is currently unclear, and requires further investigation.

In order to compensate for the high series resistance (R_S) in the devices, resulting from low activation of n-type dopants in Ge, we employed a total resistance (R_{Total} =V_D/I_D) slope-based method [103] to extract μ_{eff}, using the following formula:

$$\mu_{eff} = 1/(WQ_{INV}A) \qquad (3.2)$$

where A is the slope of the R_{Total} vs. L plots, W is the channel width and Q_{INV} is the inversion charge density. Figure 3.10 (b) shows that the correction for R_S results in about 21% enhancement in μ_{eff} extracted from the long channel (L=75 μm) devices. As expected, the enhancement is even larger (~95%) for shorter channel (L=10 μm) devices. Therefore, performance of Ge nMOSFETs fabricated in this work is limited to a large extent by their high R_S and hence is expected to be further improved by increasing the activation of dopants in the S/D regions.

3.4 SUMMARY

In this chapter, we describe development of a simple and novel approach to grow GeO_2 by RTO, which results in a low D_{it} at the Ge/high-k interface. The thermal stability of the GeO_2 passivation layer has also been investigated via material and electrical characterization. Furthermore, high-k/metal-gate Ge pMOSFETs with a RTO-grown interfacial GeO_2 layer were also fabricated. The GeO_2-passivated Ge (100) pMOSFETs show ~1.8× enhancement in hole mobility (with a peak μ_{eff} of ~175 $cm^2V^{-1}s^{-1}$) over the

control devices without GeO_2 passivation. Furthermore, a low SS of ~119 mV/decade and a high I_{ON}/I_{OFF} ratio of ~10^5 were achieved in the GeO_2-passivated devices, corroborating the passivating qualities of the RTO-grown GeO_2 interfacial layer demonstrated in this work. We have demonstrated high mobility gate-first Ge (111) nMOSFETs with a novel RTO grown, interfacial GeO_2 layer. The Ge (111) nMOSFETs show ~2× enhancement in electron mobility (with a peak μ_{eff} of ~713 $cm^2V^{-1}s^{-1}$) and ~1.6× enhancement in drive current over control Si (100) devices. A good SS of ~130 mV/decade and an I_{ON}/I_{OFF} ratio of ~10^3 were achieved. Further enhancement in device performance is expected from the optimization of S/D series resistance.

- Starting Substrate: p-Ge
- Cyclic HF clean
- RTO at 400°C for 3 min (10 slm dry O_2)
- ALD of ~8 nm Al_2O_3
- PVD of TaN
- PMA (400°C in N_2 ambient)
- FGA (400°C in forming gas)

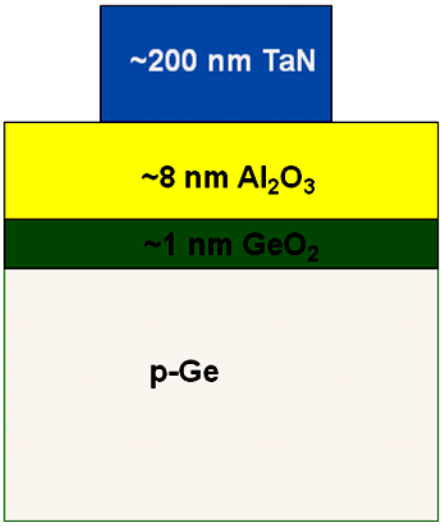


Figure 3.1: Process flow and device structure of RTO-grown GeO_2-passivated MOS devices.

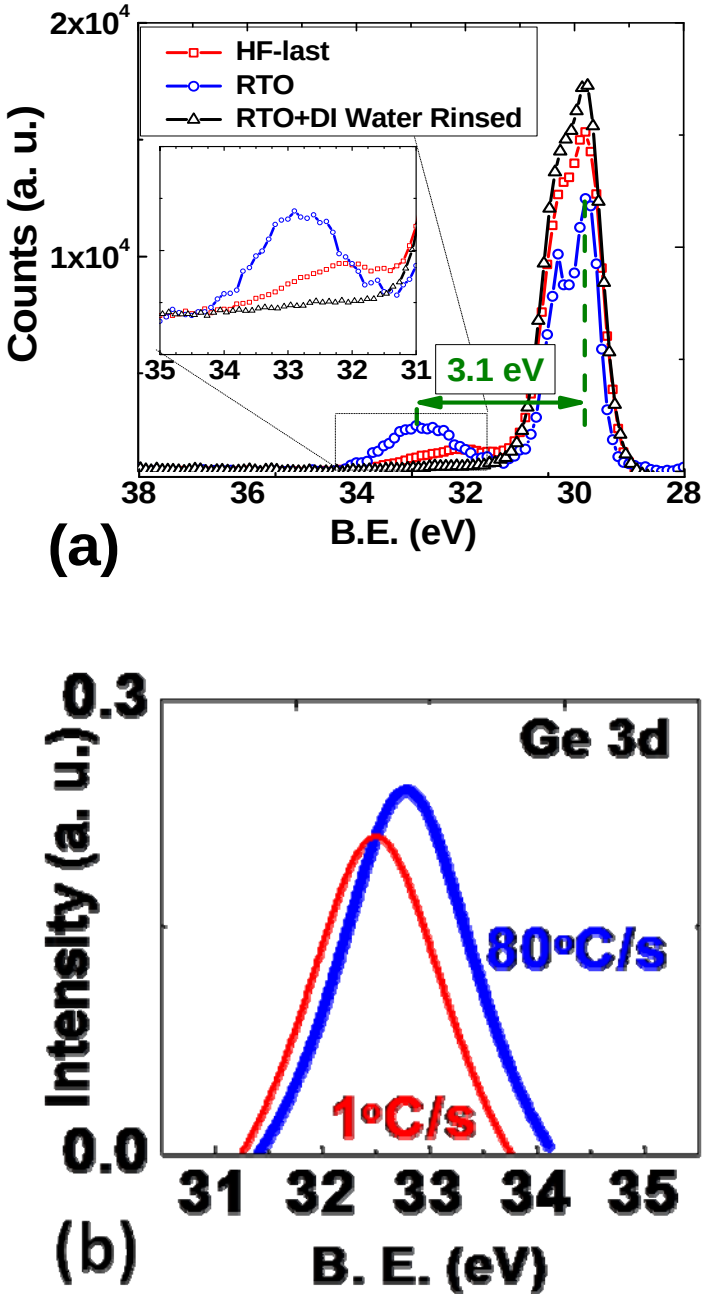


Figure 3.2: (a) XPS 3d spectra confirm the formation of GeO_2 (4^+ oxidation state at ~3.1eV) during the RTO-based passivation of Ge; (b) XPS 3d spectra of GeO_x grown using different RTO ramp rates, faster ramp reduces sub-oxide formation and thus shows advantage of RTO over conventional oxidation.

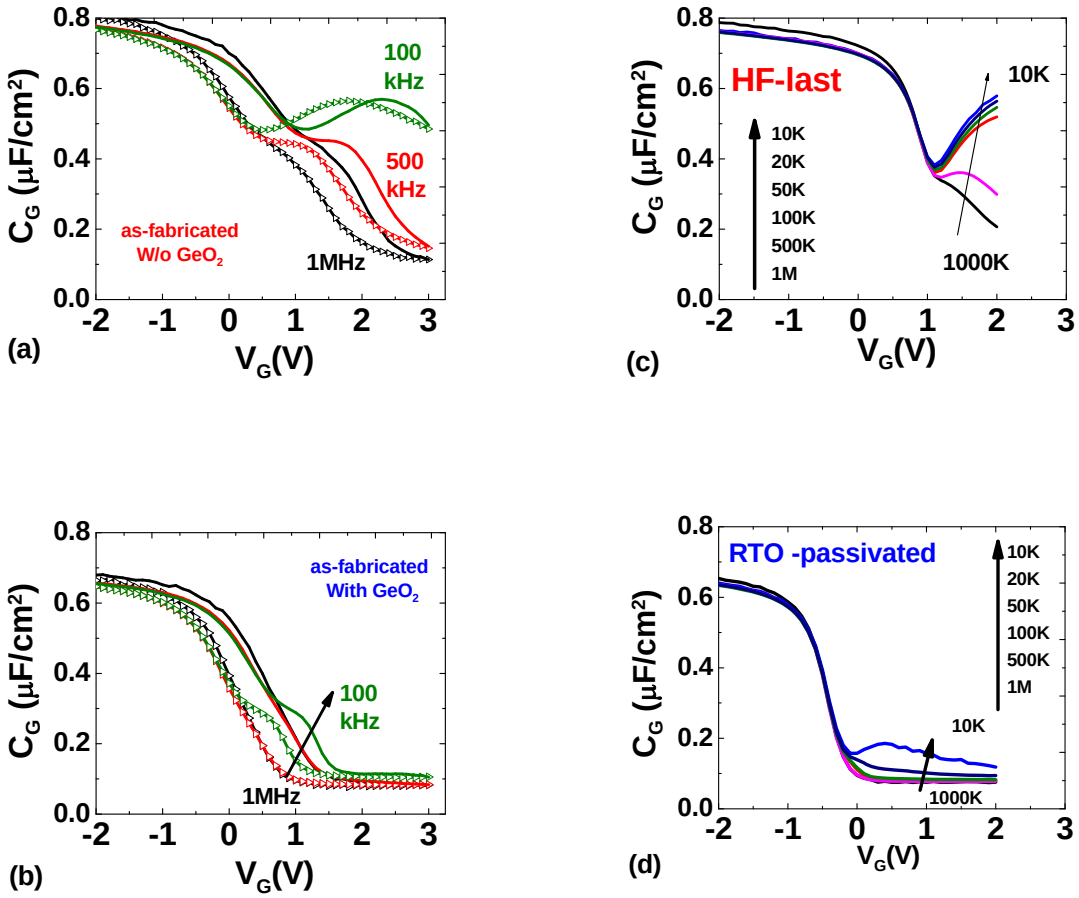


Figure 3.3: C-V characteristics of HF-last and RTO-passivated Ge MOSCAPs- (a) and (b) show the frequency dispersion characteristics of as-fabricated devices; (c) and (d) show the same for 400ºC for 5 min annealed devices. The improved C-V characterisitics of the RTO-passivated devices indicate a low D_{it} at the Ge/high-k interface.

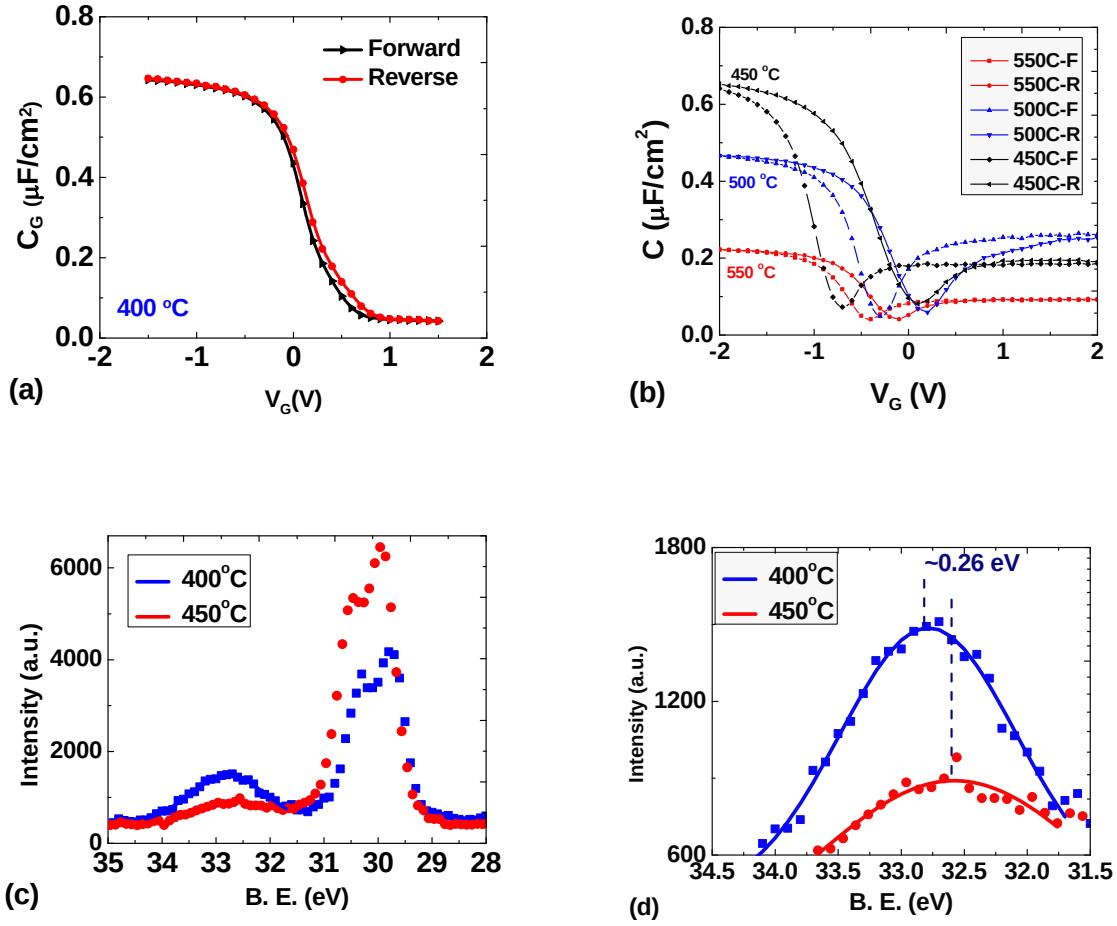


Figure 3.4: Effects of oxidation temperature on RTO-passivation: (a) and (b) C-V characteristics of the MOSCAPs with GeO_x layer grown at 400ºC show much lower hysteresis, compared to the devices with GeO_x grown at 450ºC and above; (c) and (d) XPS 3d spectra of the GeO_x layers grown at 400ºC and 450ºC, indicating presence of more 4^+ states during 400ºC oxidation.

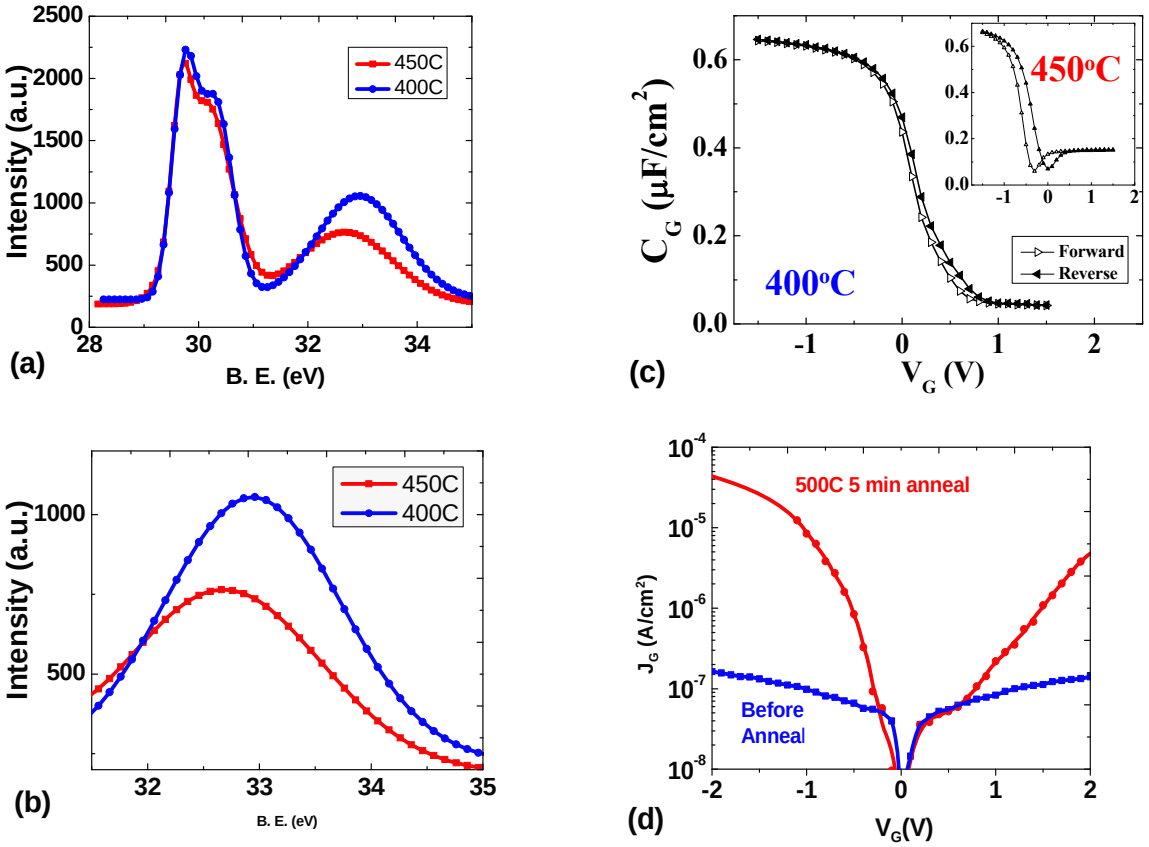


Figure 3.5: Effects of PMA at different temperatures- (a) and (b) XPS 3d spectra of GeO_x/Ge stack after 400ºC and 450ºC PMA for 5 min, showing anneal at 450ºC decomposes GeO_2 and reduces 4^+ oxidation states in the interfacial GeO_2 layer. (c) Effects of PMA temperature on C-V characteristics: the MOSCAPs annealed at 450ºC show increased hysteresis, as GeO_2-passivation is not stable above 400ºC. (d) Gate-leakage current density increases by ~1-2 orders of magnitude after 500ºC anneal for 5 min.

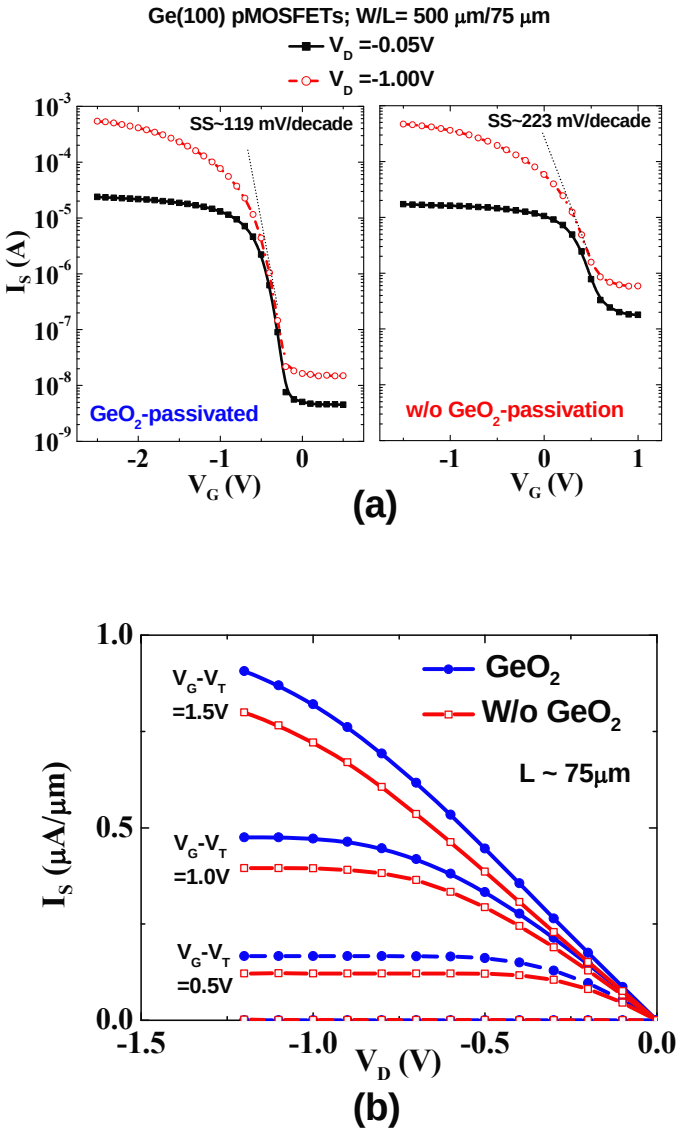


Figure 3.6: (a) I_S-V_G characteristics of Ge (100) pMOSFETs fabricated with GeO_2-passivation and without GeO_2-passivaton. The GeO_2-passivated devices show a lower SS and about 2 orders of magnitude improvement in I_{ON}/I_{OFF} ratio over their HF-last counterparts. (b) I_S-V_D characteristics of the Ge (100) pMOSFETs with and without GeO_2 passivation, showing ~1.2× enhancement in drive current while using GeO_2 passivation.

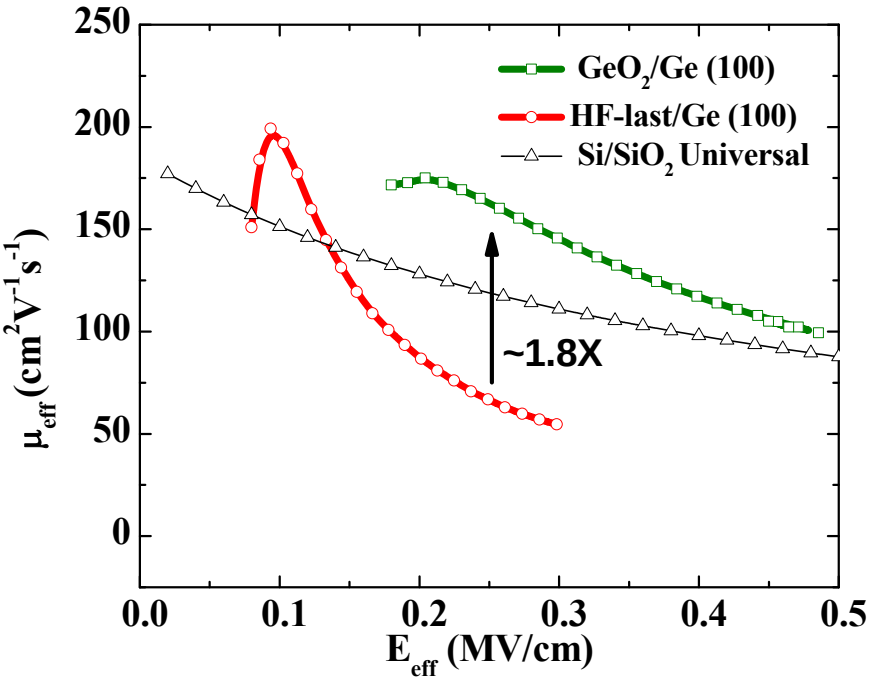


Figure 3.7: μ_{eff} vs. E_{eff} plots of Ge (100) pMOSFETs fabricated with and without GeO_2-passivation. The GeO_2-passivated devices show ~1.8× enhancement in hole mobility over their HF-last counterparts.

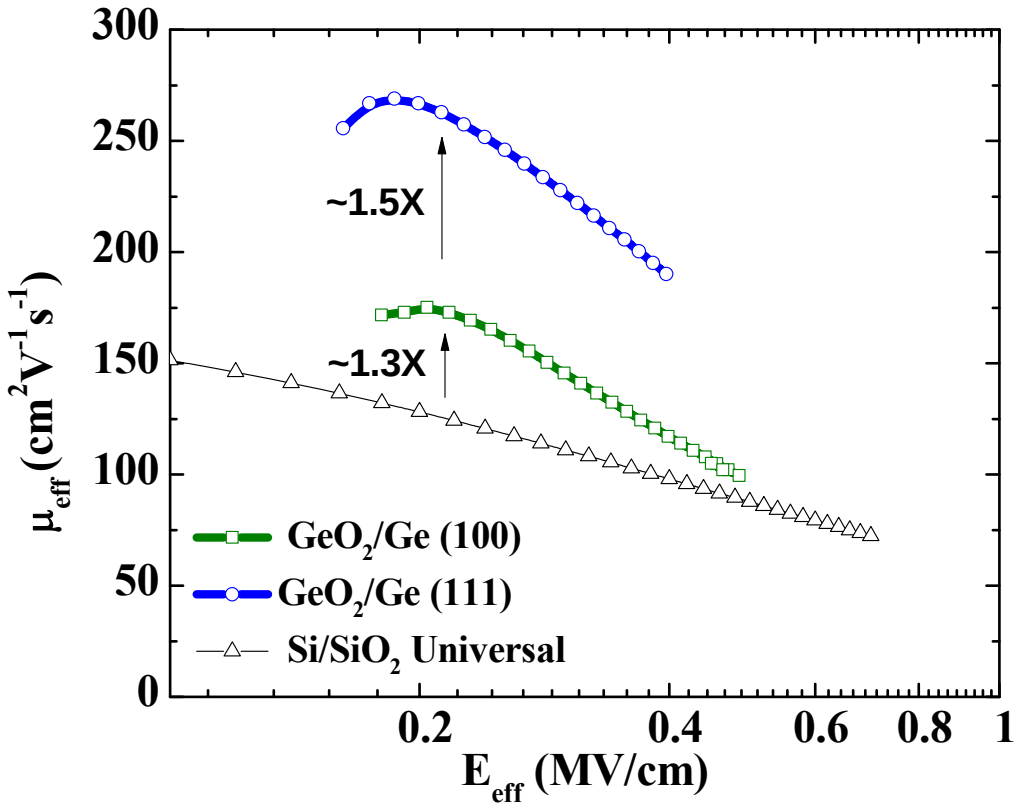


Figure 3.8: μ_{eff} vs. E_{eff} plots of GeO_2-passivated pMOSFETs fabricated on Ge (100) and Ge (111) substrates. The Ge (111) devices show ~1.5× enhancement in hole mobility over their Ge (100) counterparts. The enhancement in mobility can be attributed to two reasons – (i) higher mobility on (111) orientation, and (ii) significantly lower doping concentration in the (111) substrates (~5-40 Ω-cm), compared to the (100) substrates (~0.005-0.02 Ω-cm) used in this work.

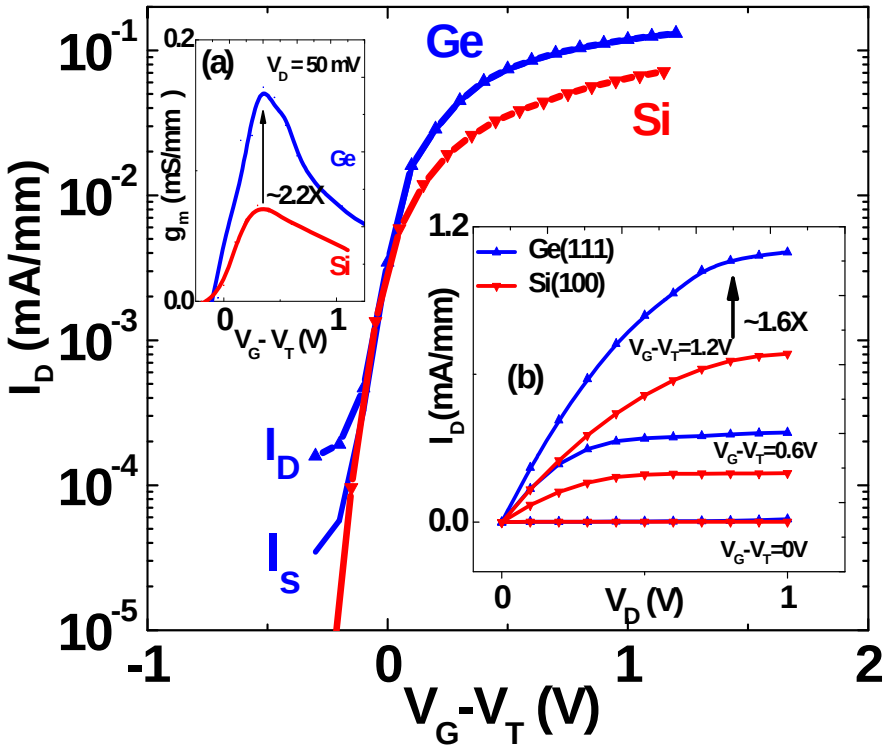


Figure 3.9: Transfer characteristics of TaN/Al_2O_3/GeO_2/Ge (111) and TaN/Al_2O_3/Si (100) nMOSFETs (W/L=500/75 μm) in linear region (at V_D = 50 mV). Inset (a) compares g_m of the same devices, where Ge nMOSFET shows ~2.2× enhancement over Si nMOSFET. Inset (b) shows output characteristics of the same devices. The GeO_2/Ge (111) nMOSFET shows ~1.6× enhancement in drive current over Si (100) nMOSFET [39].

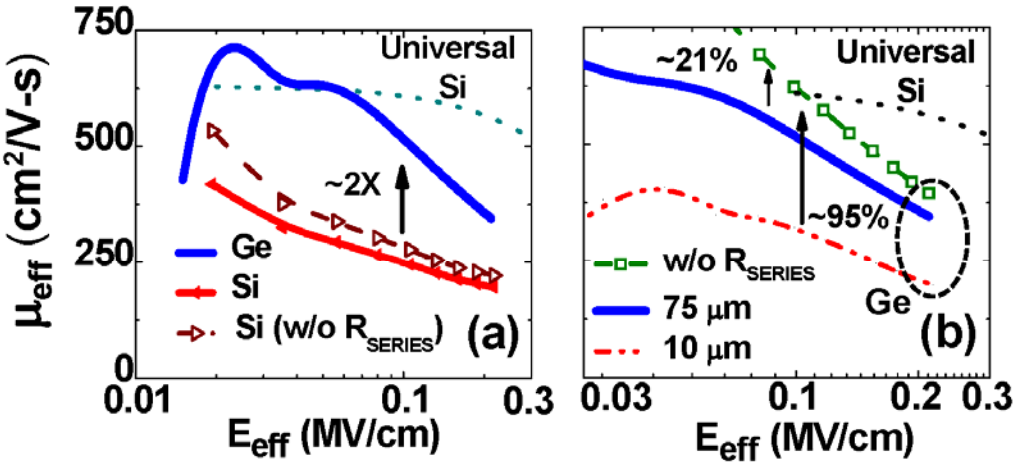


Figure 3.10: (a) μ_{eff} vs. E_{eff} plots for TaN/Al_2O_3/GeO_2/Ge (111) and TaN/Al_2O_3/Si (100) nMOSFETs extracted from long channel (L ~75 μm) devices. The Ge nMOSFETs show ~2× enhancement in μ_{eff} over the control Si nMOSFETs. Dashed line (with open symbols) shows the μ_{eff} curve of the Si control device after R_s correction. (b) Effective mobility (with R_s correction) vs. E_{eff} plots of TaN/Al_2O_3/GeO_2/Ge (111) nMOSFETs which have been extracted from the slope of R_{Total} vs. L plots for different channel length devices. Series resistance correction of a 10 μm gate length device results in ~95% enhancement in μ_{eff} [39].

Chapter 4: Investigation of Underperformance in Ge nMOSFETs

This chapter investigates temperature-dependent characteristics of the GeO_2-passivated nMOSFETs described in the previous chapter, where we introduced a simple route to grow the GeO_2 passivation layer by rapid thermal oxidation. A low mid-gap D_{it} (~10^{12} $cm^2V^{-1}s^{-1}$) was achieved at the Ge/GeO_2 interface that resulted in a high electron mobility (~715 $cm^2V^{-1}s^{-1}$, at peak) in Ge (111) nMOSFETs. Although the effective mobility achieved is comparable to that of the universal Si mobility at lower effective fields (<0.1 MV/cm), the enhancement in mobility is not as high as expected. Temperature-dependent characterization of the GeO_2/Ge (111) nMOSFETs indicates that despite significant improvement over HF-last devices, these devices still suffer from remote Coulomb scattering that limits the effective mobility in them. The ns pulsed I-V characterization performed indicates significant charge trapping in the gate dielectric that may contribute to the Coulomb-scattering and over-estimation of inversion charge density. Temperature-dependence of these devices also suggests low activation of n-type dopants, and a high density of defects in the S/D junctions that also contribute to the underperformance of Ge nMOSFETs.

4.1 INTRODUCTION

In chapter 3, we have demonstrated RTO-passivated Ge (111) nMOSFETs with a good peak effective mobility (μ_{eff}) with about 2× enhancement over Si (100) control devices. Recently, several other groups have also reported significant improvement in μ_{eff} in Ge nMOSFETs using GeO_2-based passivation layers, over their counterparts without GeO_2-passivation [37, 95]. Despite their improvement over historic devices, state-of-the-

art Ge nMOSFETs fabricated in this work and by other groups still show lower μ_{eff} than the universal Si/SiO_2 mobility, especially at higher effective fields (E_{eff}). In addition to low μ_{eff}, Ge nMOSFETs, in general, also suffer from poor sub-threshold slope (SS), low I_{ON}/I_{OFF} ratio and high off-state leakage [24, 27, 37, 95]. Such underperformance in Ge nMOSFETs are commonly attributed to the high density of interface states (D_{it}) at the Ge/high-k interface [31, 32] and to the poor n^+/p junctions due to low activation of n-type dopants in Ge [19, 24]. Among other techniques to identify the underlying mechanisms for such degradations in MOSFET structures, temperature-dependent electrical characterization of MOSFETs is a powerful non-destructive technique, as it simultaneously enables us to recognize the scattering mechanisms that may limit the μ_{eff} [104, 105] and the junction leakage mechanisms that are responsible for the off-state current [75], [90].

In this work, we have employed the technique of temperature-dependent characterization, from 300K down to 80K, and ns pulsed I-V characterization (at 300K) to investigate the underperformance of $TaN/Al_2O_3/GeO_2/Ge$ (111) nMOSFETs despite the low mid-gap D_{it} achieved at the GeO_2/Ge interface and the high intrinsic electron mobility of Ge. Temperature-dependence of different electrical properties of the fabricated MOSFETs, namely, I_{ON}/I_{OFF} ratio, I_{OFF}, SS, threshold voltage (V_T), μ_{eff}, and series resistance (R_S) , suggests that despite low mid-gap D_{it}, RTO-passivated devices still suffer from strong remote Coulomb scattering due to charge trapping in the gate stack and the interface states near the conduction-band (CB) edge. Moreover, the high R_s and poor n^+/p junctions caused by low activation of n-type dopants and inadequate removal of implantation-induced damage also contribute to the degraded behavior of these Ge nMOSFETs.

4.2 EXPERIMENTAL METHODS

In this work, we have characterized the $TaN/Al_2O_3/GeO_2/Ge$ (111) nMOSFETs from 300K down to 80K in a Lakeshore cryogenic probe station using HP 4156C semiconductor parameter analyzer and HP 4184 LCR meter for I-V and C-V characterization, respectively. The ns pulsed I-V characterization was performed at Sematech using Keithly 4200 semiconductor characterization system. The author acknowledges Michael Ramon for his collaboration to setup the pulsed I-V characterization tools at Sematech International. The details of the device fabrication steps have been described in chapter 3.

4.3 RESULTS AND DISCUSSION

4.3.1 Temperature-dependence of off-state leakage

Figure 4.1 shows the temperature-dependence of I_D-V_G characteristics of a typical RTO-passivated Ge (111) nMOSFET (W/L~500 μm/75 μm) measured in the linear region (V_D = 50 mV), from 300K down to 100K. At 300K, the devices show a moderate I_{ON}/I_{OFF} ratio of ~10^3, despite the reasonably high I_{ON} achieved using RTO-passivation and higher mobility Ge (111) substrates. As expected, the nMOSFETs demonstrate a significant reduction in I_{OFF} and improvement in I_{ON}/I_{OFF} ratio at lower temperatures. Off-state current of the devices decreases by more than 5 orders of magnitude as the operating temperature is reduced to 100K from 300k. As a result, at 100K, the devices show a high I_{ON}/I_{OFF} ratio of about 10^8 which is ~5 orders of magnitude higher than that measured at 300K. In order to investigate the dominant leakage mechanism for off-state current in these devices, the temperature-dependent data of I_{OFF} were summarized in an Arrhenius plot (Figure 4.2). The Arrhenius plot shows two distinct regions with different

slopes, indicating dominance of different leakage mechanisms at two different temperature ranges. Therefore, we have extracted two different activation energies (E_A) from different ranges of the data. From the relatively higher temperature range (>150K), an E_A of ~0.21 eV is extracted, which is significantly lower than the $E_g/2$ of Ge and thus indicates dominance of trap-assisted tunneling (TAT) [106], presumably, because of the high-density of implantation-induced damage in the S/D junctions. Even lower E_A of ~0.11 eV is extracted from lower temperatures (<150K) indicating dominance of band-to-band-tunneling [106], which may be attributed to the low bandgap of Ge.

4.3.2 Estimation of interface state densities

The reduction in I_{OFF} at lower temperatures also results in a decrease in subthreshold swing (SS). Figure 4.3(a) summarizes the SS vs. temperature data, which shows a slope of ~0.4 mV/decade/K. The SS data can be utilized to extract the D_{it} of the fabricated MOSFET devices by employing the following equation:

$$SS = 2.3\times(kT/q)\times\{1+(C_d+C_{it})/C_{ox}\} \qquad (1)$$

By using the SS data shown in Figure 4.3(a) in equation (1), we have extracted a reasonably low D_{it} of ~3×10^{12} $cm^{-2}eV^{-1}$, which is comparable to the mid-gap D_{it} extracted from the GeO_2/Ge (111) MOS devices, using conductance method at 300K (Figure 4.3(b)).

Figure 4.4(a) shows the threshold voltage (V_T) of the devices as a function of temperature. As expected, V_T increases as the temperature decreases, however, the V_T-shift (ΔV_T) as a function of temperature is much larger than that expected from an ideal case of zero interface states. Therefore, any additional shift in V_T can be attributed to the charging and discharging of the interface states. According to this approximation, D_{it} is given by the following equation,

$$D_{it} = \frac{(\Delta V_{T,ideal} - \Delta V_{T,measured})}{q} C_{ox} \qquad (2) \qquad [107]$$

where, $V_{T,ideal}$ is the theoretical V_T without considering D_{it}, and $V_{T,ideal}$ is the actual V_T measured at different temperatures. The main advantage of using eqn. (2) to extract D_{it} is that this method facilitates extraction of D_{it} closer to the conduction-band (CB) edge which plays a critical role in nMOSFET performance. Therefore, to further investigate the role of near CB edge D_{it} on the fabricated devices, we have extracted the D_{it} using (2), and summarized the data as a function of energy in Figure 4.4 (b). The plot shows a high D_{it} of ~10^{13} $cm^{-2}eV^{-1}$ near the CB edge, which is higher than that at the mid-gap by ~1-2 orders of magnitude. Such a high D_{it} near the CB-edge may cause significant charge trapping and hence strong remote-Coulomb scattering in the fabricated nMOSFETs. As a result, the Ge nMOSFETs show a relatively low mobility (compared to the universal Si mobility) because of the over-estimation of inversion charges and low drain current achieved due to the remote Coulomb scattering.

4.3.3 Pulsed I-V characterization

In order to obtain the near intrinsic I-V characterisitics of the MOSFETs without the influence from the charge trapping in the interface states and in the high-k, we have employed a unique "ns pulsed-IV technique" to minimize charge trapping when measuring the devices [108]. In principle, I-V characteristics obtained using this technique are devoid of charge trapping, if the pulses applied to the gate is so short that the traps cannot respond to it [77]. Figure 4.5 (a) shows the schematic illustration of the setup for ns pulsed I-V characterization used in this work. A pulse train with increasing amplitude was used to bias the gate and the drain current (I_d) was measured at the top of each pulse (P_W=200 ns). In addition, the rise-time and fall-time for the pulses were kept as short as possible to minimize charge trapping during rise (t_{rise}=t_{fall}= 10 ns). Figure 4.5

(b) shows the pulsed I_d-V_g characteristics of an L~10μm device measured in linear region (V_D= 0.1 mV). A significant improvement of about 1.3× was observed in drain current measured from the pulsed characterisitics over the DC characteristics. In this context, we would like to note that to probe closer to the near-intrinsic characteristics of the MOSFETs, ideally, devices with shorter channel lengths and lower series resistance (R_{SERIES}) should be used to ensure formation of a uniform inversion channel during the ultra-short pulse applied at the gate. Therefore, the actual benefit of reducing the fast-traps in the gate stack to a minimum can be much larger than the enhancement (~25%) observed from the ns pulsed I-V characterization performed in this work. Nevertheless, the pulsed I-V characterization validates the hypothesis that charge trapping in the high-k or at the high-k/Ge interface is responsible for the low mobility observed in Ge nMOSFETs. The impact of these traps on mobility degradation is two-fold. First, the mobile inversion charges available in the channel are over-estimated by conventional split-CV measurements and hence cause under-estimation of μ_{eff}. The trapped charges can further degrade the μ_{eff} in the Ge nMOSFETs as they act as the remote Coulomb scattering centers for the mobile charges in the inversion channel.

4.3.4 Temperature-dependent mobility degradation mechanisms

In order to investigate the contribution of remote Coulomb scattering to the degradation of mobility in Ge nMOSFETs, the μ_{eff} data of the RTO-passivated Ge nMOSFETs was investigated by low temperature measurements down to 77K. Figure 4.6 (a) presents the μ_{eff} vs. inversion charge density (N_{INV}) data at different temperatures for the RTO-passivated Ge nMOSFETs, which show mobility increases with decreasing temperature, likely because of reduced phonon scattering. Our observation of mobility increase with reducing temperature is in contrast with a previous study [102], where a

decrease in electron mobility was observed at lower temperature, and was attributed to increased Coulomb scattering. On the other hand, the RTO-passivated devices in this work show an increase in mobility at lower temperatures, indicating that remote Coulomb scattering is less dominant and, hence, RTO passivation may provide a pathway to higher mobility devices. However, we note that the data of Figure 4.6 (b) shows a relatively weak temperature dependence, with a negative temperature coefficient of -0.3, indicating that significant Coulomb and or surface roughness scattering are still present in these devices [92]. Therefore, although significant improvement has been achieved over other passivation schemes, optimization of the high-k stack may provide a pathway to further enhancement in device performance.

4.3.5 Low activation of n–type dopants

In addition to the charge trapping in the high-k and remote Coulomb scattering from the trapped charges, high R_S also plays a critical role towards the underperformance of Ge nMOSFETs. Therefore, to decouple the effects of R_S and the poor gate stack, the mobility data shown in Figure 4.6 were carefully corrected for R_S using total-resistance (R_{Total}) slope-based method [103]. The R_S correction performed at different temperatures reveals an interesting phenomenon of increase in R_S with decrease in operating temperatures (Figure 4.7(a)). Therefore, it is critical to do the correction for R_S throughout the temperature range, while determining the mobility degradation mechanisms from the temperature-dependence of mobility data. This is evident from the mobility data shown in Figure 4.7(b), with and without R_S correction, as the enhancement in mobility due to reduced phonon-scattering can be clouded by the increase in R_S and hence can be misconstrued as stronger Coulomb scattering. Such an increase in R_S at lower temperatures is indicative of non-degenerately doped S/D region and/ a large

Schottky barrier between the S/D region and the metal contact because of strong Fermi-level pinning at the metal/n-Ge interface. The impact of this high R_S on device performance is also evident from room-temperature characteristics, as the correction for R_S results in about 20% enhancement in μ_{eff}, extracted even from a long channel (L=75 μm) device. Such a high R_S and high I_{OFF} in our devices are presumably related to inadequate removal of ion-implantation damage during S/D activation at a low temperature (400ºC). In the gate-first process flow employed in this work, we kept the highest processing temperature to 400ºC, as the GeO_2-passivation layer is not stable above 400ºC. It may be noted that several other groups have also observed similarly high R_S in Ge nMOSFETs fabricated using different thermal budget or process flows [24, 27, 40]. Therefore, a pathway to achieve high performance n^+/p junctions with a high activation of n-type dopants and a low defect density is required towards integration of Ge nMOSFETs in future CMOS devices.

4.4 SUMMARY

We have investigated performance degradation mechanisms in RTO-grown GeO_2-passivated Ge (111) nMOSFETs through temperature-dependent and pulsed I-V characterization. The devices show relatively high D_{it} near the CB edge and significant charge trapping in the gate stack. Temperature dependence of the electrical characterisitics of the devices identify strong remote Coulomb scattering as the dominant cause for mobility degradation and TAT due to the implantation-induced damage as the root cause of high off-state leakage in these devices. Further enhancement in device performance is expected from the optimization of the gate stack and the S/D junctions.

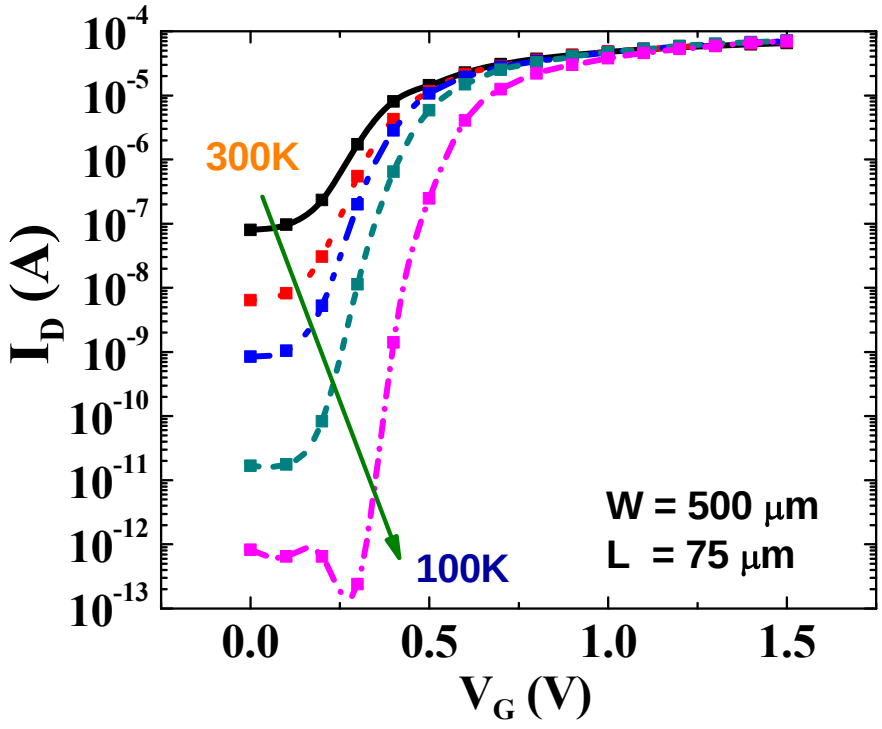


Figure 4.1: Transfer (I_D-V_G) characteristics of RTO-passivated Ge nMOSFETs in linear region (V_D=50 mV), measured at different temperatures at 50K intervals. Off-state leakage reduces by about 5 orders of magnitude at 100K.

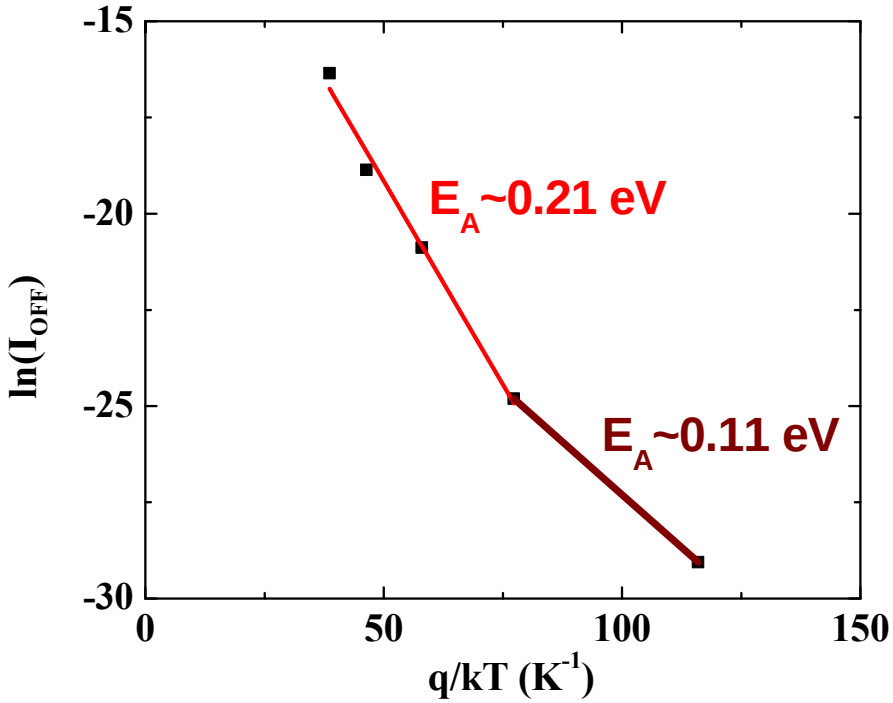


Figure 4.2: Arrhenius plot of I_{off} measured at different temperatures in linear region (V_D =50 mV). The low activation energy of ~0.21eV indicates that these Ge devices suffer from trap-assisted tunneling and band-to-band tunneling, presumably due to the high-density of defects in the S/D junction.

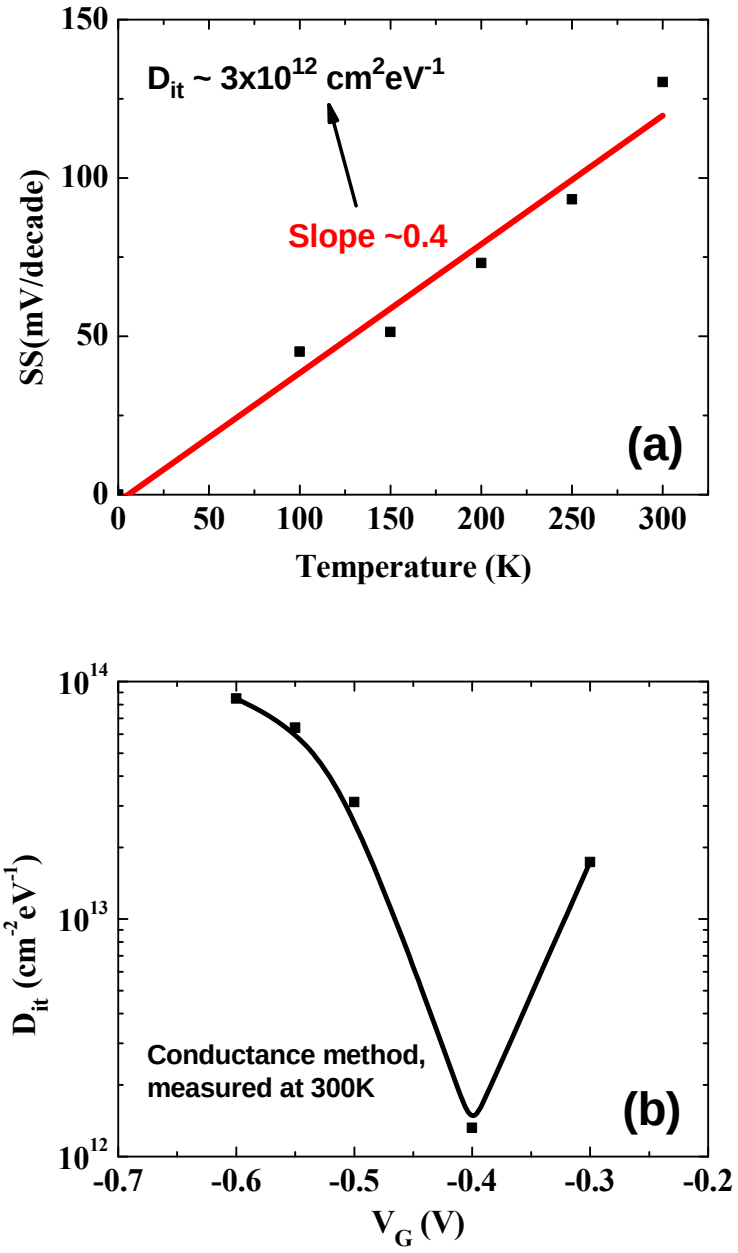


Figure 4.3: (a) Subthrehold-slope vs. temperature plot of RTO-passivated Ge (111) nMOSFETs in linear region (V_D = 50 mV). The slope of the SS vs. T plot indicates a low D_{it} of ~3×10^{12} $cm^{-2}eV^{-1}$ at the GeO_2/Ge interface. (b) D_{it} vs. V_G plot of the same devices, measured using conductance-method at 300K, showing a mid-gap D_{it} of ~10^{12} $cm^{-2}eV^{-1}$ similar to the D_{it} measured using the SS-method.

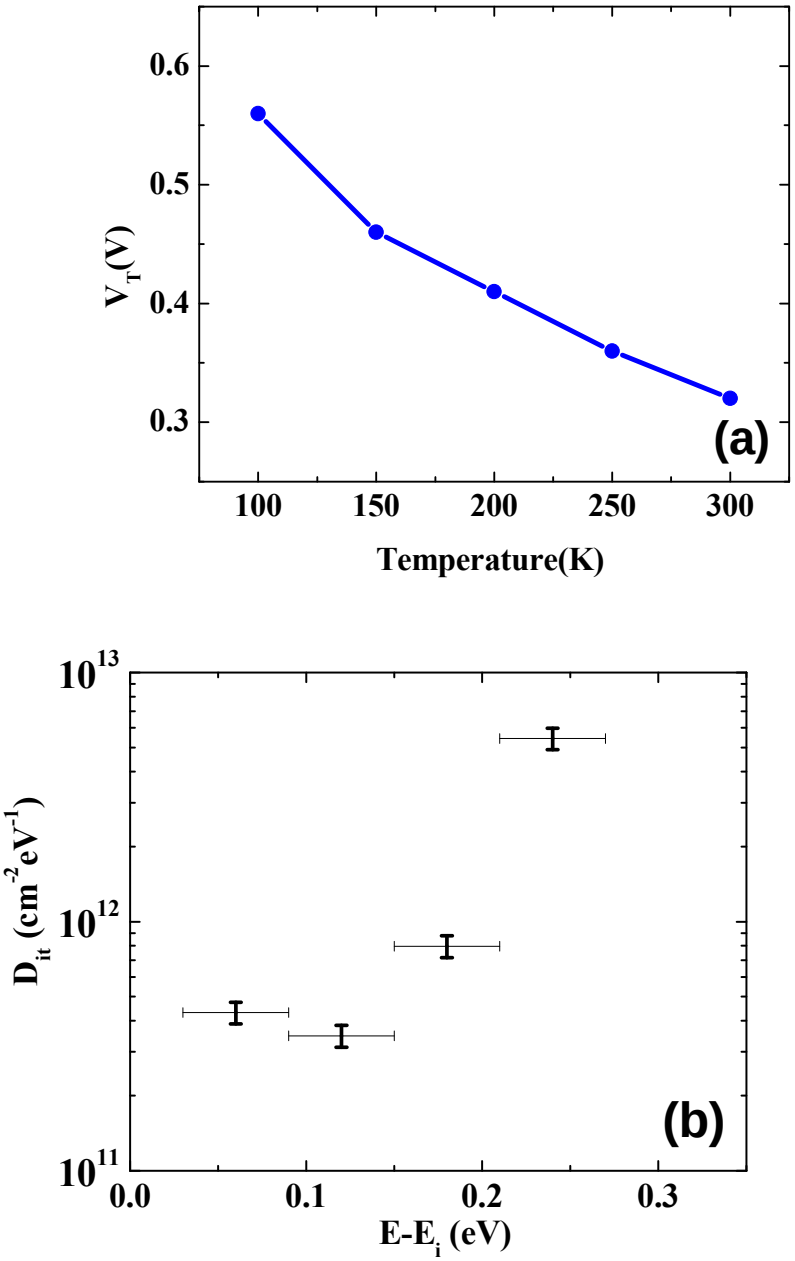
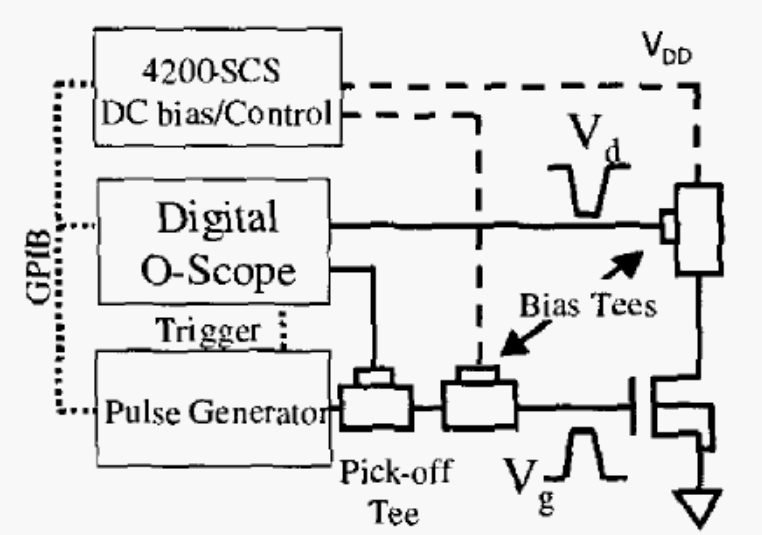
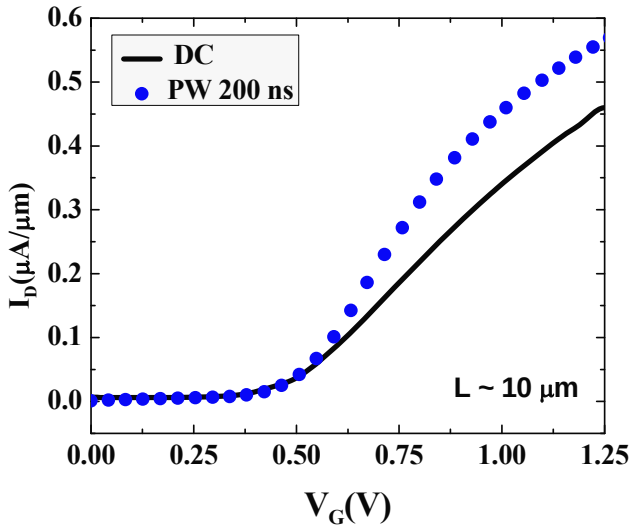


Figure 4.4: (a) Threshold voltage as a function of operating temperature; (b) D_{it} vs. E-E_i plot extracted from the temperature-dependence of V_T-shift, showing a high D_{it} of ~10^{13} near the conduction-band edge.



(a)



(b)

Figure 4.5: (a) Schematic illustration of the setup used for ns pulsed I-V measurements [77]. (b) Pulsed I_d-V_g characteristics of the GeO_2/Ge (111) nMOSFETs measured using gate pulses with increasing amplitude and a fixed pulse-width of 200 ns, showing ~30% enhancement in linear I_D over the DC characteristics, in linear region (V_D=100 mV). This enhancement indicates a high density of charge traps in the gate stack.

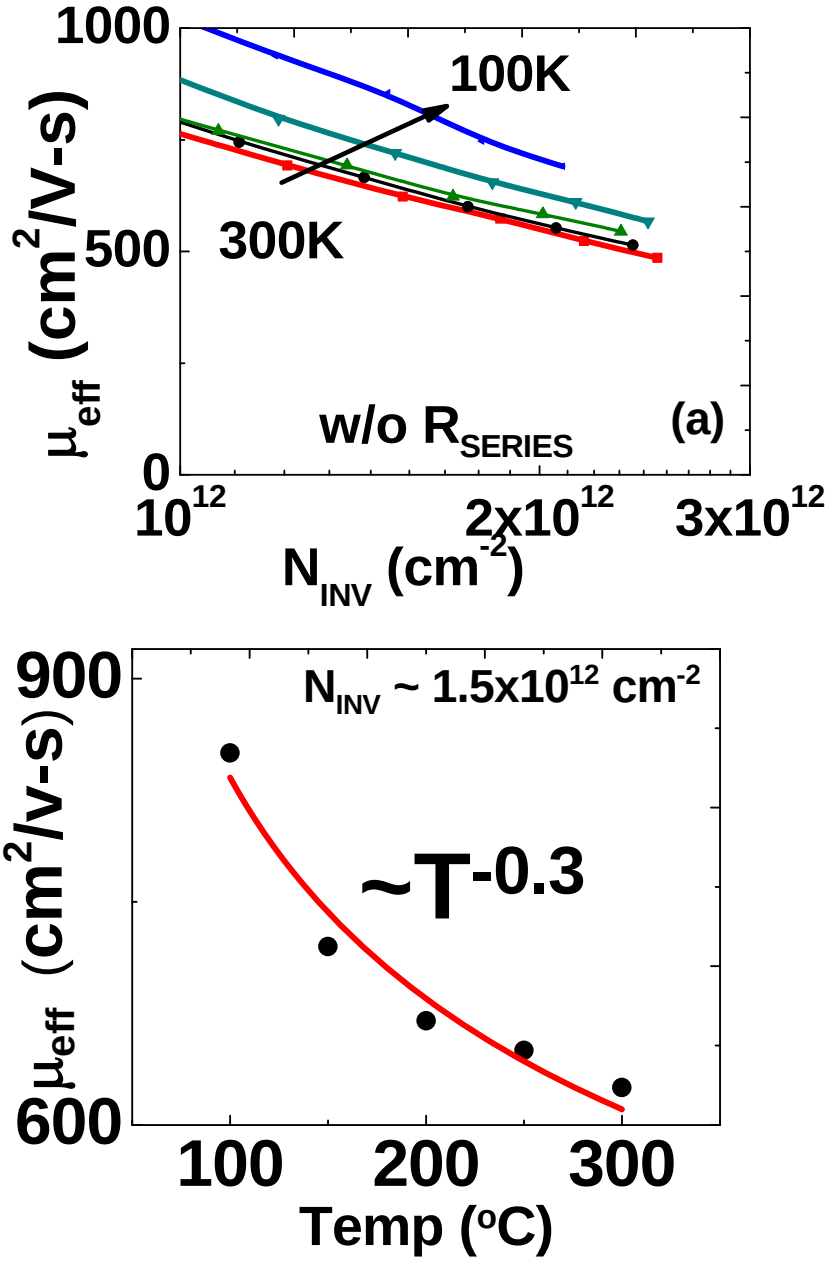


Figure 4.6: (a) Temperature-dependence of μ_{eff} vs. N_{INV} curves of the RTO-passivated Ge (111) nMOSFETs after R_{SERIES} correction, (b) μ_{eff} vs. Temperature, showing a negative temperature-coefficient of -0.3, indicating reduction in phonon scattering at lower temperatures.

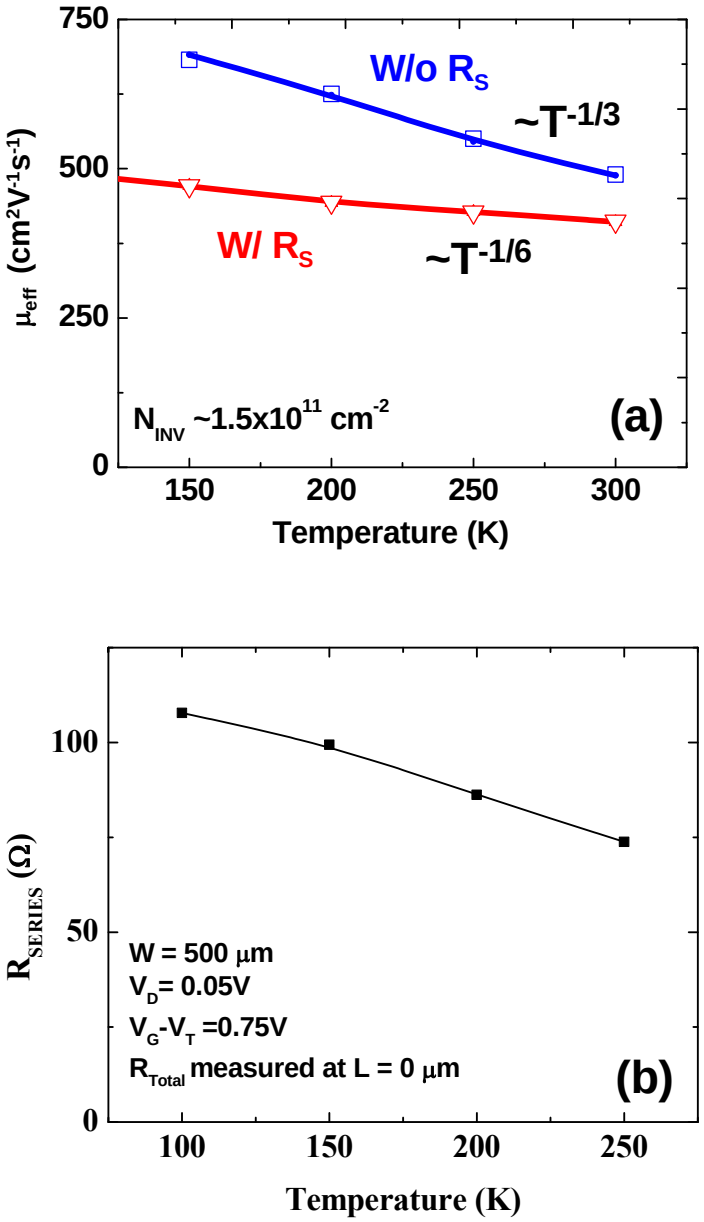


Figure 4.7: (a) Temperature-dependence of μ_{eff} vs. N_{INV} of RTO-passivated Ge (111) nMOSFETs with and without R_{SERIES} correction, (b) R_{SERIS} of the Ge nMOSFETs as a function of operating temperature. The benefit of reduction in phonon-scattering at lower temperatures may be negated to a large extent by the increase in R_{SERIES} at lower temperatures.

Chapter 5: High Performance Ge nMOSFETs with n^+/p Junctions Formed by "Spin-on Dopants"

This chapter describes fabrication and characterization of high mobility Ge nMOSFETs using a simple approach to form n^+/p junctions by rapid thermal diffusion of "spin-on dopants" to avoid implantation damage. These junctions show a high I_{ON}/I_{OFF} ratio (~10^{5-6}) and an ideality factor of ~1.03, indicating a low defect density in the junction, whereas, ion-implanted junctions show higher I_{off} (by ~1-2 orders) and a larger ideality factor (n~1.45). Germanium (100) nMOSFETs with diffusion-doping and GeO_2-passivation show a high I_{ON}/I_{OFF} ratio of ~10^{4-5}, a low SS of 111 mV/decade, and a high μ_{eff} (679 $cm^2V^{-1}s^{-1}$ at peak). The diffusion-doped devices also show lower (~1 order) GIDL, and higher (~1.3×) drive current of ~12 μA/μm in a L~20 μm device at a gate overdrive of 2V and V_D=1V, compared to the ion-implanted devices. Moreover, diffusion-doped Ge (111) nMOSFETs show even higher μ_{eff} (970 $cm^2V^{-1}s^{-1}$ at peak) and ~1.5× enhancement over diffusion-doped Ge (100) devices and surpasses the universal Si mobility at low effective fields[5].

5.1 INTRODUCTION

As discussed in previous chapters, the underperformance of Ge nMOSFETs is widely attributed to the high interface state density (D_{it}) near the conduction band edge [31], and poor n^+/p junctions due to low activation and fast diffusion of n-type dopants in Ge [24, 41]. Recently, several promising passivation schemes using GeO_2-based gate dielectrics were introduced, which show low D_{it} [40, 95], however, the realization of

[5] Part of this chapter is reproduced with permission from [109], © 2011 IEEE.

good n^+/p junctions in Ge still remains challenging [38, 40, 42, 110]. In addition to low activation, typical n^+/p junctions formed by conventional ion implantation also suffer from implantation-induced damage that cause high reverse junction leakage [38], and may cause charge trapping near the source/drain (S/D) junctions [43]. Other than ion implantation, there are a few alternative approaches to form n^+/p junctions in Ge. Among them, solid source diffusion (SSD) was proposed to avoid fast diffusion of dopants resulting from the implantation defects [44]. Recently, gas-phase doping of As [46] and SSD of Sb [111] have been used to fabricate n^+/p junctions in Ge with a low I_{OFF} and a good I_{ON}/I_{OFF} ratio, demonstrating the merits of avoiding implantation damage.

In this work, we demonstrate a simple approach to form high performance n^+/p junctions in Ge without ion implantation by rapid thermal diffusion of P from "Spin-on Dopants" (SOD). Here, we investigate P as an n-type dopant to achieve higher activation because of its higher solid solubility in Ge than Sb and As. In addition, we have introduced rapid thermal diffusion to achieve shallower junctions. This diffusion-based approach avoids implantation-induced damage and hence results in junctions with a high I_{ON}/I_{OFF} ratio and a low ideality factor (n). For MOSFET fabrication, a thin GeO_2 passivation layer was incorporated in the gate stack to combine the benefits of low D_{it} at the Ge/GeO_2 interface with the low defect density of the SOD junctions. The GeO_2 passivation layer was grown by rapid thermal oxidation (RTO), a simple approach we recently demonstrated [39]. In addition, nMOSFETs on Ge (111) orientation have been fabricated to utilize its higher electron mobility over Ge (100) [96]. The electrical activation of the n^+ layer was investigated by spreading resistance probe (SRP) analysis and the crystalline quality was investigated by Raman spectroscopy. The author acknowledges the collaboration of Jason Mantey for performing the Raman spectroscopy and helping in device fabrication, and Emmanuel Onyegam for helping in process

optimization. The SOD-doped devices show improved junction characteristics and ~1.3× enhancement in drive current over control ion-implanted devices. The superior performance of the SOD-doped devices demonstrates that SOD may provide a simple route to form better n^+/p junctions in Ge and hence achieve high mobility in Ge nMOSFETs while maintaining a good I_{ON}/I_{OFF} ratio.

5.2 DEVICE FABRICATION

First, SiO_2 was deposited on cyclic HF-cleaned Ge wafers and dummy gates were patterned for selective diffusion. A Phosphorus-doped SOD (from Filmtronics, Inc.) was spun on the patterned Ge wafers to form n^+/p junctions. The wafers were then baked at 200ºC to evaporate solvents from the SOD. The baked wafers were immediately transferred to a rapid thermal system to perform the dopant diffusion, at ~700ºC for 10s. After diffusion, the SOD layer and the dummy gate were stripped off by HF dip. The diode fabrication was completed by forming Ni contacts to the n^+ region via e-beam evaporation. For MOSFET fabrication in a gate-last approach, a thin GeO_2 passivation layer was grown by RTO after SOD and dummy gate removal. Immediately after RTO, ~8 nm Al_2O_3 and ~200nm TaN were deposited as gate dielectric and gate metal, respectively. After etching the TaN to form ring-shaped gates, about 40 nm Ni was deposited as S/D contacts to complete the MOSFET fabrication. On the other hand, control MOSFETs were fabricated with S/D junctions formed by implantation of P^+ ions at a dose of 1.5×10^{15} cm^{-2} (at 50 keV), followed by activation anneal at 550ºC for 10s.

5.3 RESULTS AND DISCUSSIONS

5.3.1 SOD-doped n^+/p junctions

Figure 5.1(a) shows the SRP data of SOD-doped Ge demonstrating an electrical activation of ~7×10^{19} cm^{-3} (at the peak), which is ~2-3× times higher than that achieved in the control ion-implanted sample. Moreover, this activation is also higher than that achieved in [112] (~5×10^{19} cm^{-3}), one of the best activations reported by ion implantation in literature. However, the activation using SOD is lower than that achieved using recently reported techniques of laser annealing [113] or co-implantation [114], which also significantly reduced the residual implantation damage. The higher activation achieved in the SOD-doped layers is presumably indicative of a lower defect density in the n^+-Ge layers. The lower defect density in the SOD-doped layer was verified by Raman spectroscopy (λ~532 nm) shown in Figure 5.1(b). The SOD-doped Ge shows Raman intensity close to pristine Ge, whereas, the implanted Ge shows much lower intensity, indicating significant residual damage even after solid-phase-epitaxy.

Figure 5.2 shows the I-V characteristics of the n^+/p diodes formed by SOD or implantation on p-Ge (~0.1 Ω-cm), where the diffusion, implantation and activation conditions were optimized independently to increase the I_{ON}/I_{OFF} ratio . In the SOD-doped junctions, a lower defect density is expected near the depletion region. As a result, these junctions show ~2 orders of magnitude lower reverse junction leakage compared to their counterparts formed by ion implantation (1×10^{15} cm^{-2} at 30 keV). While the implanted diodes show a high ideality factor (n ~1.45), the SOD diodes show a low n of ~1.03, which indicates that junction leakage in SOD-doped diodes is diffusion-dominated. In order to verify diffusion-dominated leakage in SOD-doped junctions, the I-V characteristics of the diodes were measured at elevated temperatures (290K-360K) and an activation energy (E_A) of ~0.67eV was obtained from an Arrhenius plot of the I_{off}

data at V_R=0.5V(Figure 5.3). This E_A is close to the bandgap of Ge which corroborates the diffusion-dominated leakage current and low defect density in the SOD junctions.

5.3.2 Ge nMOSFETs with SOD-doped junctions

The I_S-V_G characteristics (Figure 5.4(a)) of the SOD-doped nMOSFETs show a good I_{ON}/I_{OFF} ratio of ~10^{4-5} with a low off-state leakage of ~3×10^{-10} A/μm, thanks to the low defect density in the S/D junctions. The low I_{OFF} and RTO-passivation results in a low SS of 111 mV/decade that translates to a low D_{it} of ~2×10^{12} cm^{-2}, and is comparable with the mid-gap D_{it} measured from the MOSCAPs by quasi-static C-V method at 290K(~9×10^{11} cm^{-2}). Such a low D_{it} observed after MOSFET fabrication warrants the gate-last approach adopted in this work, as Ge nMOSFETs fabricated in a conventional gate-first flow suffer from severe degradation in D_{it} due to high temperature processing (>400 ^oC) during S/D formation. The SOD devices also exhibit an order of magnitude lower GIDL than the implanted devices in saturation region as shown in the I_D-V_G characteristics (Figure 5.4(b)), presumably because of the lower defect density in the gate overlap region, which reduces trap-assisted tunneling. Furthermore, the I_D-V_D characteristics of the SOD-doped devices demonstrate a high drive current of ~12 μA/μm at a gate over-drive of 2V in an L~20 μm device at V_D = 1.5V and ~1.3× enhancement over implanted devices (Figure 5.4(c)). As expected, SOD-doped devices fabricated on higher mobility (111) orientation show an additional ~33% enhancement in drive current over their (100) counterparts with SOD-doping (not shown).

The μ_{eff} vs. effective field (E_{eff}) data (Figure 5.5) are extracted from linear I_D-V_G and split C-V characteristics and are corrected for series resistance and channel length by total resistance-slope method [103]. The SOD devices show a high μ_{eff} (679 $cm^2V^{-1}s^{-1}$ at

peak) and ~1.15× enhancement over ion-implanted devices, presumably because of reduced charge trapping near the S/D junctions [43]. The Ge (111) nMOSFETs with SOD show an additional ~1.5× enhancement over Ge (100) nMOSFETs, with a peak μ_{eff} of ~970 $cm^2V^{-1}s^{-1}$ and surpasses the universal Si/SiO_2 mobility at low fields (E_{eff} < 0.2 MV/cm).

5.4 SUMMARY

In summary, we demonstrate an implantation damage free approach to form n^+/p junctions in Ge by rapid thermal diffusion of SOD. High I_{on}/I_{off} ratio, low I_{off} and near unity ideality factor have been achieved using this approach, thanks to the relatively low defect density in the junctions formed by SOD. The Ge nMOSFETs with SOD show a high I_{on}/I_{off} ratio with a high μ_{eff} of ~679 $cm^2V^{-1}s^{-1}$ at peak. Moreover, Ge (111) nMOSFETs fabricated with SOD show ~1.5× enhancement over Ge (100) devices, demonstrating suitability of SOD approach on this high mobility orientation.

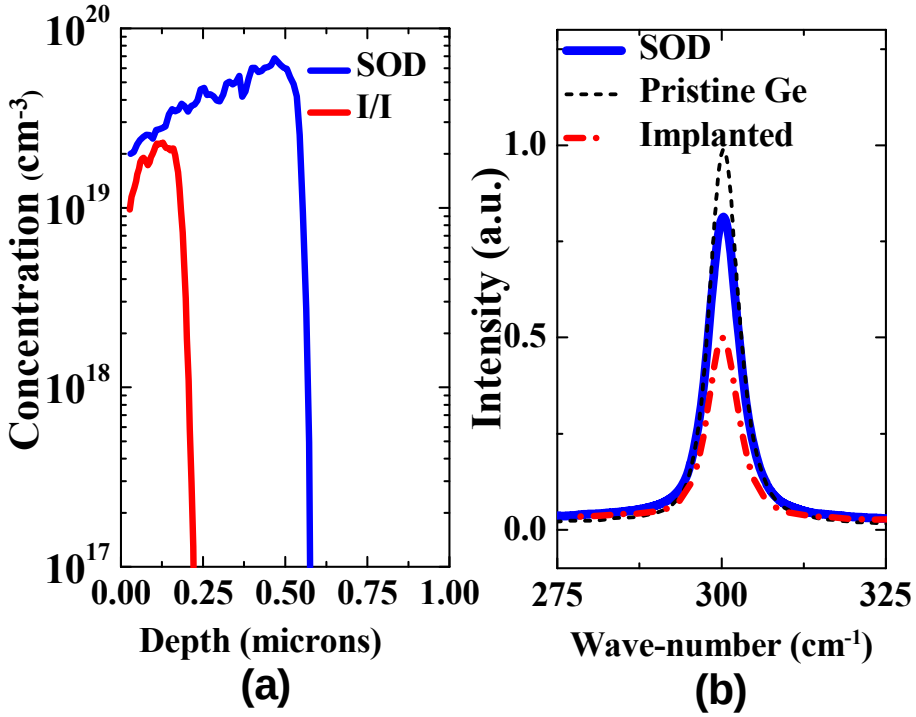


Figure 5.1: (a) SRP depth profile data of P-doped n^+-Ge layers formed by diffusion from SOD, showing a high activation of ~7×10^{19} cm^{-3}. (b) Raman spectroscopy analysis of P-doped Ge samples, indicating better crystalinity of the SOD-doped Ge, compared to the ion-implanted Ge.

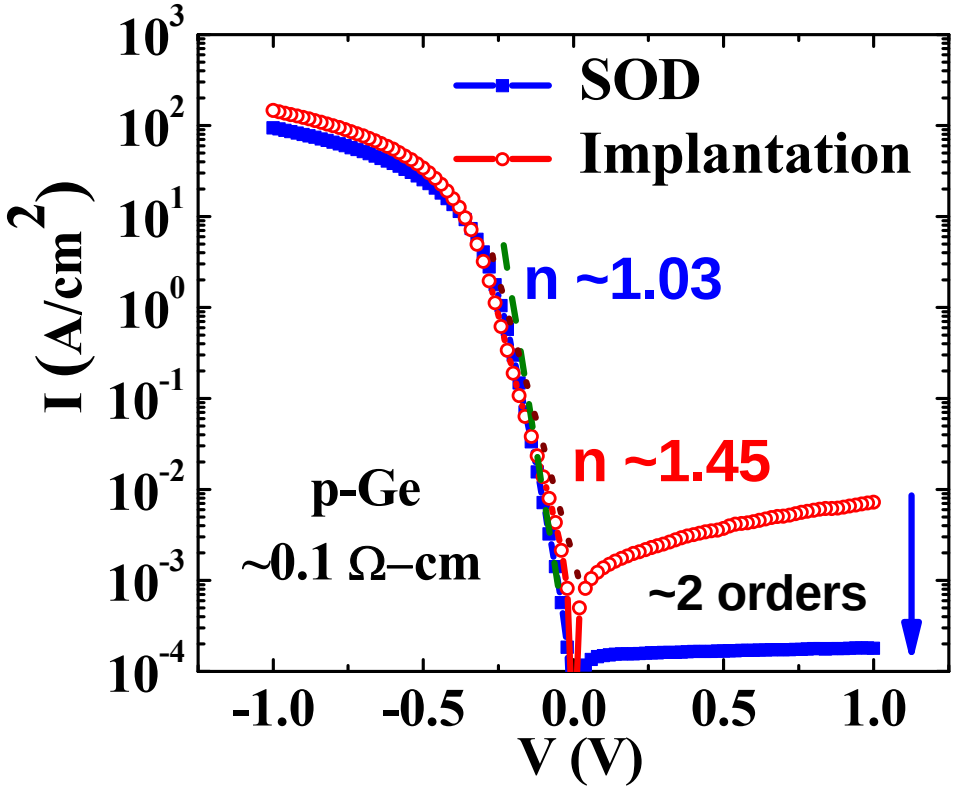


Figure 5.2: I-V characteristics of Ge n^+/p diodes. SOD reduces I_{off} by ~1-2 orders of magnitude and shows a near unity ideality factor of~1.03, indicating a low defect density. On the other hand, the ion-implanted diodes show a high ideality factor of 1.45, indicating a higher defect density [109].

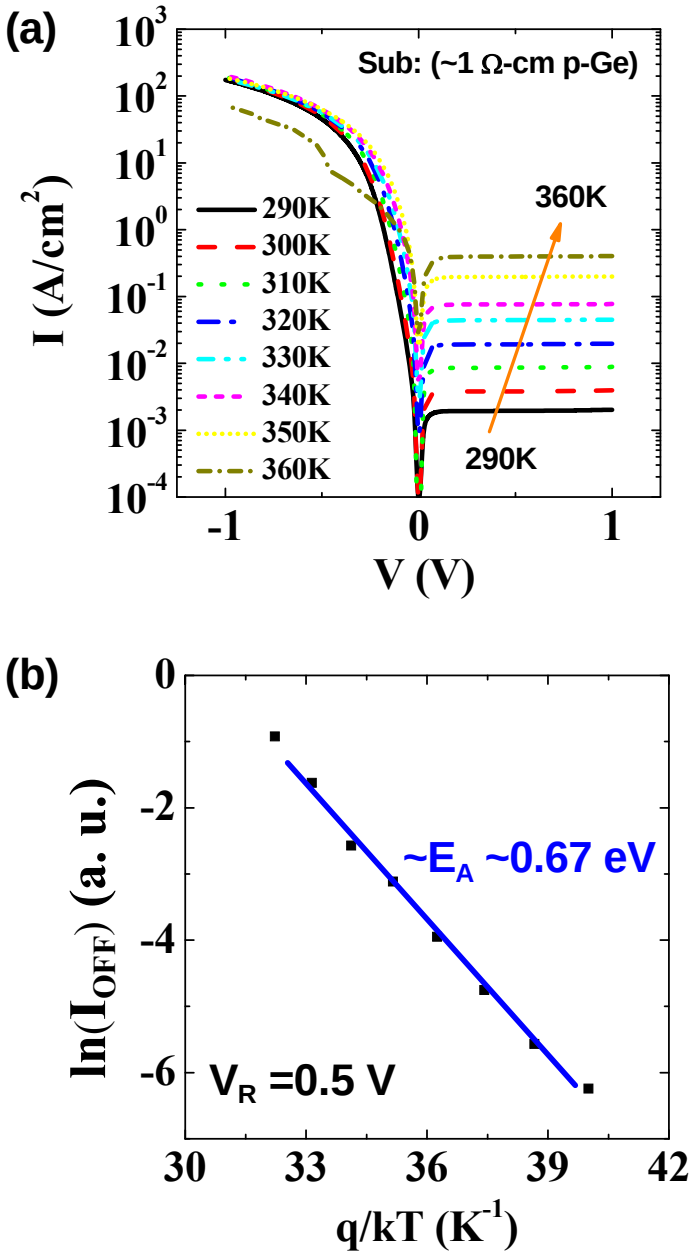


Figure 5.3: (a) Temperature-dependent I-V characterisitics of Ge n^+/p junctions fabricated on p-Ge(100) substrates (~1 Ω-cm) formed by SOD, measured at elevated temperatures (290K-360K). (b) The Arrhenius plot of I_{OFF} (at V_R=0.5V) shows an E_A of ~0.67 eV, equal to the bandgap of Ge, suggesting diffusion-dominant reverse junction leakage, that indicates lower defect density in the junctions formed by SOD.

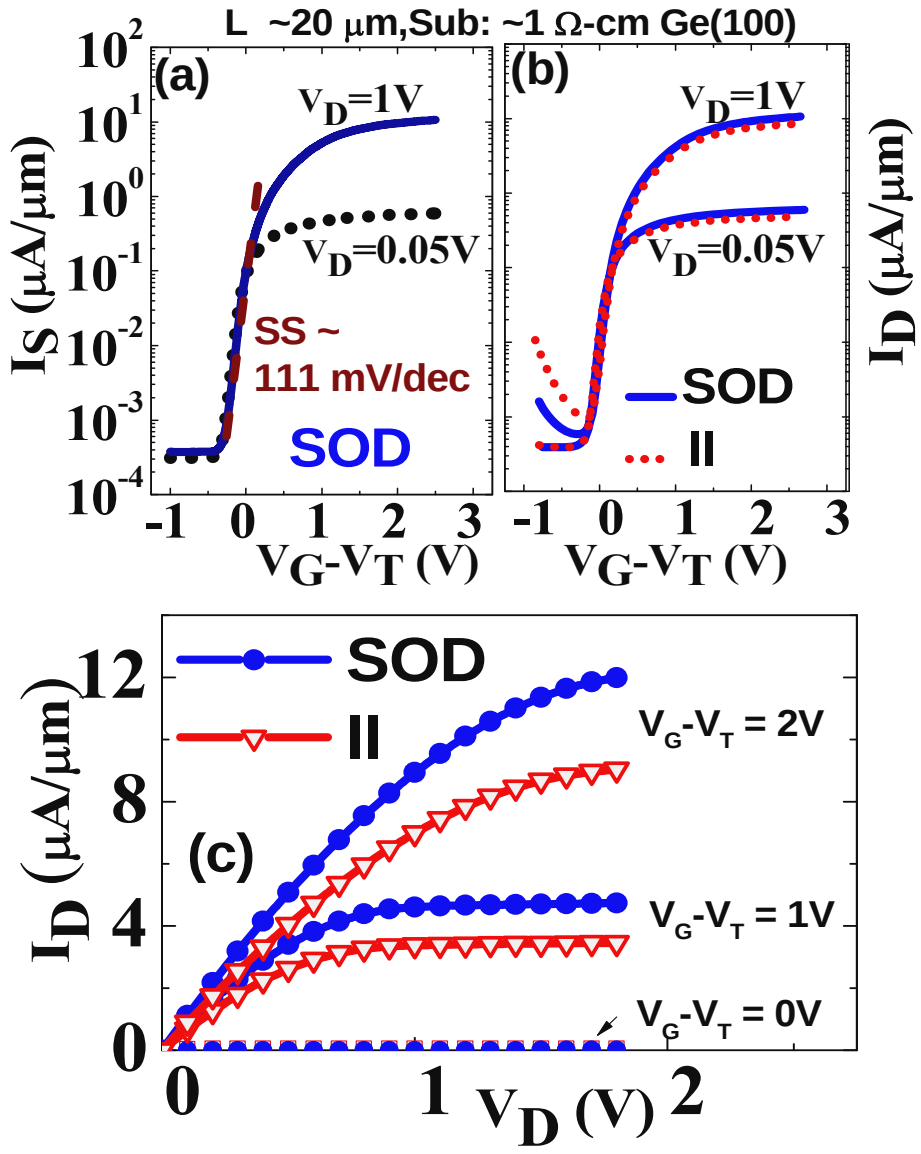


Figure 5.4: (a) I_S-V_G characteristics of Ge (100) nMOSFETs with SOD-doped junctions show high I_{ON}/I_{OFF} ratio and a low SS, indicating low defect density in the S/D and low D_{it} at the GeO_2/Ge interface. (b) I_D-V_G characteristics of Ge (100) devices; the SOD-doped devices show ~1 order lower GIDL at V_D=1V. (c) I_D-V_D characteristics of Ge (100) nMOSFETs at V_G-V_T intervals of 1V; The SOD-doped devices show ~1.3× enhancement in drive current over ion-implanted devices [109].

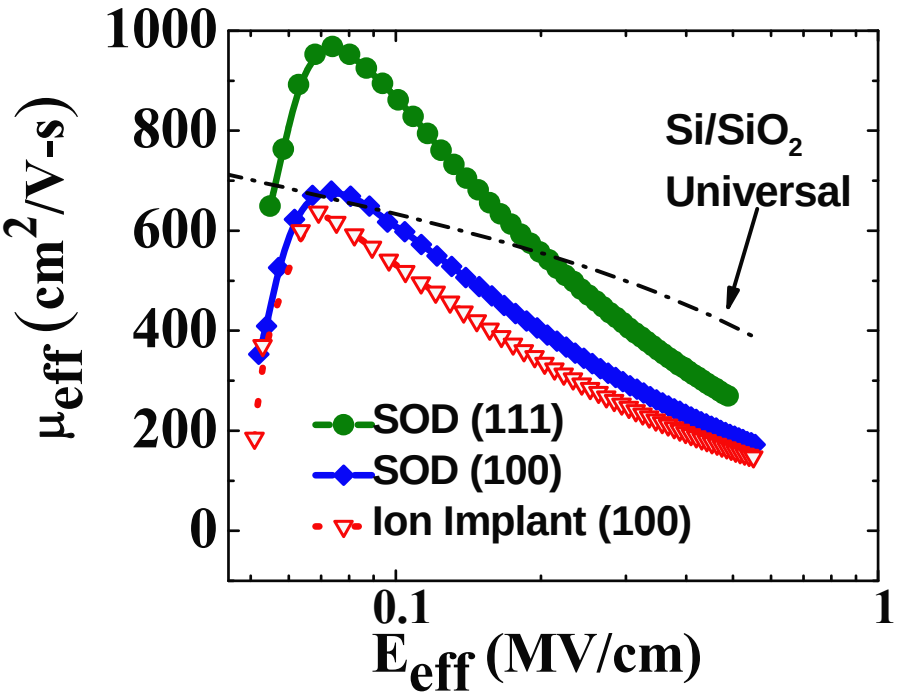


Figure 5.6: μ_{eff} vs. E_{eff} plots for Ge nMOSFETs after R_{SERIES} correction extracted from long channel devices (L ~5-20 μm); the devices with SOD demonstrate a high μ_{eff} (679 $cm^2V^{-1}s^{-1}$at peak), which is higher than that of the implanted devices, presumably because of reduced charge trapping near the S/D junctions. The SOD-doped Ge (111) devices show an additional ~1.5× enhancement over Ge (100) devices (~970 $cm^2V^{-1}s^{-1}$ at peak), and surpass universal Si mobility at low fields [109].

PART II: BEYOND CMOS MATERIALS AND DEVICES

Chapter 6: Ferromagnetism in Mn-Implanted Epitaxially Grown Ge:C on Si (100)

This chapter investigates ferromagnetism in Mn^+-implanted epitaxial Ge:C (C <0.5%) films grown on Si. Implantation of Mn^+ ions resulted in Ge:C:Mn films with an effective concentration of about 16at%, 12at%, 6at% and 2at%. Magnetic characterization performed using superconducting quantum interference device (SQUID) show that the samples with higher Mn concentration (>= 6at%) are ferromagnetic, while the sample with lower Mn concentration (2at%) is paramagnetic. Transmission electron microscopy and synchrotron grazing incidence X-ray diffraction study show that the Mn^+-implanted region is amorphous and we believe this amorphous phase makes Ge:C:Mn ferromagnetic, as recrystallization transforms it into a paramagnetic material[6].

6.1 INTRODUCTION

As discussed in chapter 1, the main challenge with dilute magnetic semiconductor material thin films, including widely studied (III,Mn)V systems, is that the Curie temperature (T_c) is still well below room temperature. Several groups are trying to develop new DMS materials with a Curie temperature higher than room temperature. One promising material system is Mn-doped Ge because of its compatibility with Si processing. Theoretical studies show that Mn dopants prefer to occupy substitutional sites

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in a crystalline Ge lattice [115] and one can optimize Mn doping by adding other codopants [116, 117] . Theoretical modeling also predicts enhanced magnetic properties and higher solubility of Mn-doped amorphous Si and Ge systems [118]. There have been a number of reports on experimental studies of ferromagnetism of Mn-doped Ge systems [61-63], with some groups reporting Curie temperatures near room temperature for nanowires [64] and above room temperature for nanocolumns [65] and quantum dots [66]. Several growth techniques have been employed to produce epitaxial Mn-doped Ge films: low temperature MBE [61, 62] [63], ultrahigh vacuum thermal coevaporation [119], and high energy Mn-ion implantation into single crystal Ge [120]. Besides all of these methods, chemical synthesis techniques have been also used to grow $Ge_{1-x}Mn_x$ nanowires [64] and MBE has been used to grow Mn-rich nanocolumns [65] and quantum dots [66] embedded in Mn-poor matrix. Near room temperature T_c observed in nanowire, nanocolumn and quantum dot suggest confinement is helpful to increase T_c and hence thin Ge films doped with Mn may also be promising for higher T_c.

One of the major challenges with these $Ge_{1-x}Mn_x$ studies is the presence of different phases in those samples. For example, Sugahara *et al*. [63] have shown the presence of a Mn-rich amorphous phase in MBE grown crystalline epitaxial films and have claimed that the amorphous phase is responsible for ferromagnetism in MBE grown $Ge_{1-x}Mn_x$ films. Amorphous $Ge_{1-x}Mn_x$ films, grown by ultra high vacuum thermal co-evaporation, also show the presence of embedded nanocrystals [119]. For high energy Mn-ion implanted Ge samples, Ottaviano *et al*. have reported the presence of ferromagnetic Mn_5Ge_3 nanoparticles [120]. Also for high energy Mn-ion implanted Ge samples [121], transmission electron microscope (TEM) images clearly show presence of two distinct ion-implanted regions in as-implanted samples. Moreover, these Mn-ion

implanted studies did not conclusively exclude the possibility of defect-induced ferromagnetism as the origin of ferromagnetic behavior [122].

In this work, we have fabricated Ge:C:Mn thin films formed by low energy Mn^+ implantation on Ge:C-on-Si substrates. This approach is attractive from the perspective of CMOS integration because of the CMOS compatibility of the epitaxial Ge:C films. Here we investigate the following critical questions regarding the Mn-doped Ge system: a) What are the magnetic properties of crystalline Mn-doped Ge phase without any second phase? b) What are the magnetic properties of amorphous Mn-doped Ge phase? c) What are the magnetic properties of Mn-ion implanted Ge samples after recrystallization?, and d) What is the origin of ferromagnetism in Mn-ion implanted Ge samples?

To answer these questions we characterized the films using superconducting quantum interference device (SQUID), secondary ion mass spectroscopy (SIMS), transmission electron microscopy (TEM), Grazing-incidence X-ray diffraction (GI-XRD) analysis, X-ray absorption spectroscopy (XAS), and X-ray magnetic circular dichroism (XMCD) analysis. The author acknowledges invaluable contributions of the collaborators in this project: Dr. Samaresh Guchhait for SQUID and XPS measurements, Texas Instruments for SIMS and TEM analysis, Stanford Synchrotron Radiation Lightsource (SSRL) for GI-XRD and XMCD analysis, and Advanced Light Source (ALS) in Berkeley for XAS measurements. The author also thanks Dr. Domingo Ferrer and Dr. Moon J. Kim (UT-Dallas) for their help with the TEM and GI-XRD analysis, respectively. Our as-implanted samples are amorphous and there is no significant second phase of Ge and Mn. The amorphous Mn-doped Ge phase is ferromagnetic, while the annealed crystalline phase is paramagnetic. We also report a basic magnetic phase diagram of these amorphous Ge:C:Mn-on-Si films.

6.2 EXPERIMENTAL DETAILS

The Ge layers were grown on (100) Si wafers in a custom-built cold wall ultra high vacuum chemical vapor deposition (UHV-CVD) system. A trace amount of C was introduced in Ge during the epitaxial growth process to facilitate 2-D growth of Ge directly on Si surface and also to reduce bulk extended defects in the epitaxial Ge layer [74, 75]. The details of Ge:C growth methodologies are described in chapter 2. The growth temperature (~460°C) and pressure (7 mTorr) were optimized to grow thick ~250 nm Ge:C film used in this study, while maintaining a smooth surface (rms roughness < 0.5 nm) and good crystallinity (verified by XRD and X-TEM analysis).

To incorporate Mn into Ge:C, Mn^+ ions were implanted into a 4-inch diameter epitaxial Ge:C-on-Si wafers at 20 keV with four different doses: a) $1.5\times10^{16}/cm^2$, b) $1.1\times10^{16}/cm^2$, c) $5.5\times10^{15}/cm^2$, d) $2.5\times10^{15}/cm^2$ at 7^o tilt angle. These samples so obtained will be denoted as A, B, C and D, respectively. During ion implantation, samples were kept at 300^oC to minimize crystal damage. Under these conditions, the Mn projected range is about 17 nm and the straggle is about 9 nm, as determined by SRIM simulations. Figure 6.1 is a low-resolution cross-sectional TEM image of sample A, showing Mn-implanted region (~20 nm) and epitaxial Ge:C layer (~250 nm) on top of Si (100) substrate. After ion implantation, the samples were cut into 6 mm × 6 mm squares for magnetic property measurements, and for TEM analysis, while 1 cm × 1 cm squares were used for GI-XRD, XPS, and SIMS studies. Throughout the experiments, Teflon tweezers were always used in order to minimize spurious ferromagnetic impurity incorporation during sample handling [123]. The pieces were also cleaned by ultrasonication in acetone for 2 minutes, followed by isopropyl alcohol (IPA) to remove the surface contaminants. Isochronal (for 90s) and isothermal (at 300^oC) anneals were performed in an N_2 ambient to study the structural evolution of these ion implanted films.

6.3 RESULTS AND DISCUSSIONS

6.3.1 SIMS analysis

Dynamic SIMS was used to determine Mn and O profiles in all the four samples (Figure 6.2). Actual total Mn^+-implant doses were calculated from Mn SIMS profiles and were found to be in correlation with the nominal implant doses. These SIMS profiles also show the average concentration of Mn in samples A, B, C and D to be approximately $9.3\times10^{21}/cm^3$, $7.5\times10^{21}/cm^3$, $3.0\times10^{21}/cm^3$, and $7.8\times10^{20}/cm^3$, respectively. It may be noted that the peak position of the Mn profiles for different dosage are not exactly the same. The exact mechanism that is causing such behavior is not very clear at the moment, however, we hypothesize that concentration-dependent diffusion or error in estimation of SIMS depth-profile due to different Mn-content may have lead to such uncertainty. Nevertheless, we believe that the ferromagnetic properties of these films do not depend on the precise Mn peak location, but more on the Mn concentration and total dose, which were confirmed by SIMS measurements. The SIMS profiles for Oxygen indicate an O-rich layer in the top 3 nm of all the samples. For example, the oxygen SIMS profile of sample A is shown in the inset of Figure 6.2.

6.3.2 Magnetic Properties of Mn-implanted Epitaxial Ge Thin Films

Figure 3 shows the in-plane temperature dependent magnetic moment measurements performed at 0.2 Tesla down to 5 K, using a superconducting quantum interference device (SQUID) magnetometer by Dr. Guchhait in the department of physics. Each magnetization curve is made up of magnetic field-cooled and zero-field-cooled data, which show a spin-glass phase at very low temperatures. It was found that temperature-dependent field-cooled and zero-field-cooled magnetic moments diverge below a certain temperature, which is defined as the spin-glass temperature. A spin-glass

phase is expected as it is likely that many structural defects and binary phases of Ge and Mn are present at this high Mn concentration [124]. Curie temperatures are estimated from these temperature-dependent magnetic moment measurements by defining it as the temperature at which magnetic moment goes to zero. Temperature-dependent magnetization (Figure 6.3) and magnetic hysteresis measurements (Figure 6.4) show that the samples A, B and C are ferromagnetic, while the sample with lowest dose (2%) is paramagnetic. Moreover, Curie temperatures (170 K, 145 K, and 130 K, respectively) and saturated magnetization (20.0 emu/cm^3, 9.5 emu/cm^3, and 5.9 emu/cm^3, respectively) of ferromagnetic samples A, B and C scale with the total Mn dose, as shown in the inset of Figure 6.3. Temperature-dependent magnetic hysteresis shows that the coercive field is significant only below a certain temperature, known as the superparamagnetic temperature. Above this superparamagnetic temperature, the coercive field is very small as shown in the inset of Figure 6.4. For sample A, superparamagnetic temperature is about 20 K. Figure 6.5 summarizes the dependence of the Curie temperature, spin-glass temperature and superparamagnetic temperature as a function of Mn-implant dose for the samples studied.

To further address the role of Mn atoms on the magnetic properties, XAS and XMCD measurements were performed. The details of these studies were discussed in [78]. The XAS spectrum (not shown) indicates that there is hardly any long-range crystalline order in the Mn-rich region and the Mn atoms in the amorphous region are isolated double donors with localized magnetic moments of 2.5 Bohr magnetons per Mn atom. In comparison, the average magnetic moment measured by the SQUID magnetometer is only 0.23 Bohr magnetons per Mn atom for sample A. This clearly indicates that only a fraction of Mn atoms (about 10%) are ferromagnetically coupled with each other. This is expected for an ion-implanted sample, which has a near Gaussian

distribution of Mn concentration, as evident from the SIMS profile (Figure 6.2). Presumably, Mn atoms at the tail of this distribution are not ferromagnetically coupled to each other, thus giving less than expected magnetization. On the other hand, the XMCD signal (shown in [78]) decreases with increasing temperature and reaches a constant value at about 150 K. The remaining XMCD contribution does not change significantly above 150 K and can be attributed to the paramagnetic phase, while the increase in XMCD signal below 150K indicates temperature-dependent ferromagnetic order. Thus, the XMCD data, along with the XAS data, indicate that the ferromagnetic ordering observed in our samples is not defect-induced magnetic ordering [122].

6.3.3 Structural Characterization of Mn-implanted Epitaxial Ge Thin Films

In order to better understand the origin of the ferromagnetism in Mn-implanted epitaxial Ge:C films, high resolution transmission electron microscopy (HR-TEM), XPS and GI-XRD studies were performed. Cross-sectional HR-TEM images of as-implanted samples indicate that the implanted region is amorphous, without any precipitation, above the end of implant range (Figure 6.6(a)). The top surface of the recrystallized Ge:C:Mn layer is oxygen-rich, as indicated by photoemission electron microscopy (PEEM) data (not shown). Besides, the XPS spectra (data not shown) also indicate the presence of oxygen in the top 3 nm of the as-implanted samples; both Ge and Mn in the top 3 nm are partially oxidized. This result agrees well with oxygen SIMS profiles. Moreover, below top 3 nm, XPS spectra of both Ge and Mn of our as-implanted Mn-doped Ge samples are indistinguishable from their respective pure elemental XPS spectra.

Rapid thermal annealing experiments were performed to monitor the evolution of Ge:Mn microstructure and its relation to magnetization and Curie temperature. Isothermal annealing of sample A at 300^{o}C shows that as the annealing time increases,

saturation magnetization decreases, but Curie temperature remains the same, as shown in Figure 6.7 (a). Moreover, the normalized temperature-dependent magnetization plots of as-implanted and annealed (for different times) samples superimpose on each other (Figure 6.7 (b)). These results suggest that the phase responsible for ferromagnetism in Ge:C:Mn, is not changing but its amount (per unit sample volume) decreases with increasing annealing time. Furthermore, the sample annealed at 500^{o}C for 90 seconds recrystallizes completely and becomes paramagnetic. Figure 6.6 (a) and (b) show high resolution TEM images of an as-implanted film and one annealed at 600^{o}C for 90 seconds. It is clear from these cross-sectional TEM images that the as-implanted film shows an amorphous region above the end of implant range; whereas the annealed film shows a completely recrystallized implanted region. Recrystallization of the top surface during anneals performed at higher temperatures are also verified by GI-XRD analysis performed in collaboration with UT Dallas, as shown in Figure 6.6 (c). As expected, the top surface of the as-implanted and 300°C annealed samples are amorphous, whereas, that of the sample annealed at higher temperature is crystalline. Therefore, it seems that ferromagnetism is associated with the presence of an amorphous phase, rather than a crystalline phase. Further, the ferromagnetism is not related to the presence of crystalline Ge_3Mn_5 or other ferromagnetic Ge and Mn alloys. A similar effect has also been observed by Sugahara *et al.* [63], where they intentionally grew an amorphous layer of Mn-doped Ge by MBE on SiO_2.

Synchrotron GI-XRD experiments (shown in Figure 6.8) were also performed to investigate the crystalline structure of sample A with further precision, at Stanford Synchrotron Radiation Lightsource (SSRL) beamline 2-1 at 10 keV X-ray energy. For a 10 keV photon source and incident angles of 0.10^{o}, 0.15^{o} and 0.20^{o}, the estimated X-ray penetration depths are about 2.4 nm, 2.8 nm and 3.6 nm, respectively. For very low

incident angles (0.10^o and 0.15^o), GI-XRD data show the presence of (110) GeO_2 and (102) MnO_2 peaks. These two oxide phases have also been observed in TEM and XPS studies on the surface of implanted region. For higher incidence angle of 0.20^o, XRD data show presence of (111), (222) and other higher order Ge peaks, however, all of them are very broad. Moreover, there is also a very weak and broad XRD peak that matches with the strongest peak of many known binary alloys of Ge and Mn (for example Ge_2Mn_5, Mn_2Ge, GeMn, $GeMn_3$, Ge_8Mn_{11} and Ge_3Mn_5). However, the concentrations of these phases are very low compared to the amorphous Ge:Mn phase. Nevertheless, the broad Ge diffraction peaks for all three incident angles suggest that there is no long-range order in the Mn-implanted Ge region, as has also been observed in the HR-TEM images.

6.4 SUMMARY

We have investigated ferromagnetism in Mn-implanted epitaxially grown Ge on Si (100) substrates. The GI-XRD data and TEM images show that Mn-implanted Ge thin films are amorphous, without any significant second phase. We believe that this amorphous phase is responsible for ferromagnetism in these films. Curie temperature and saturated magnetic moment are monotonic function of Mn implant dose above 6at%. Isothermal annealing of Ge:Mn films at 300^oC for up to 1200 seconds decreases the saturated magnetization but does not change the Curie temperature, suggesting that the volume of magnetic phase slowly decreases with annealing time at 300^oC. High temperature annealing results in recrystallization and transforms the material into a paramagnet, which further supports that the amorphous phase is the source of ferromagnetism in the Ge:C:Mn films investigated in this work.

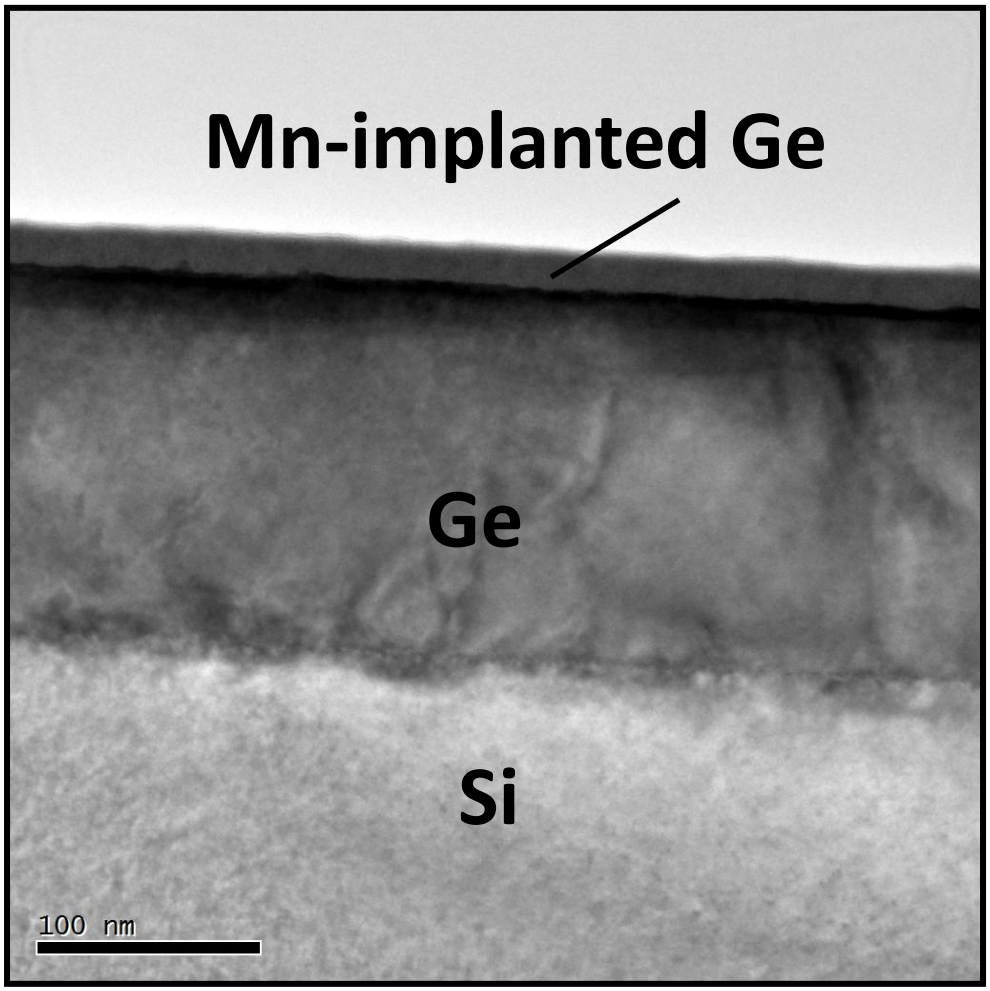


Figure 6.1: Low resolution X-TEM image of as-implanted sample A, showing Mn-implanted region and epitaxially grown Ge on top of Si (100) wafer [78].

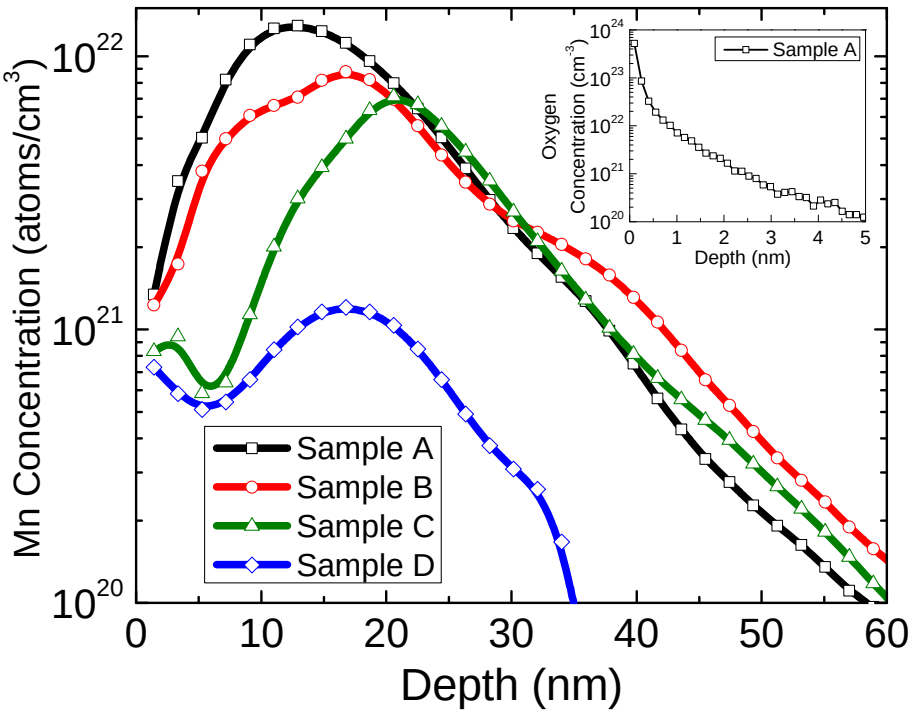


Figure 6.2: Manganese concentration SIMS profiles of four as-implanted Ge:Mn samples. Inset shows oxygen SIMS profile of sample A [78].

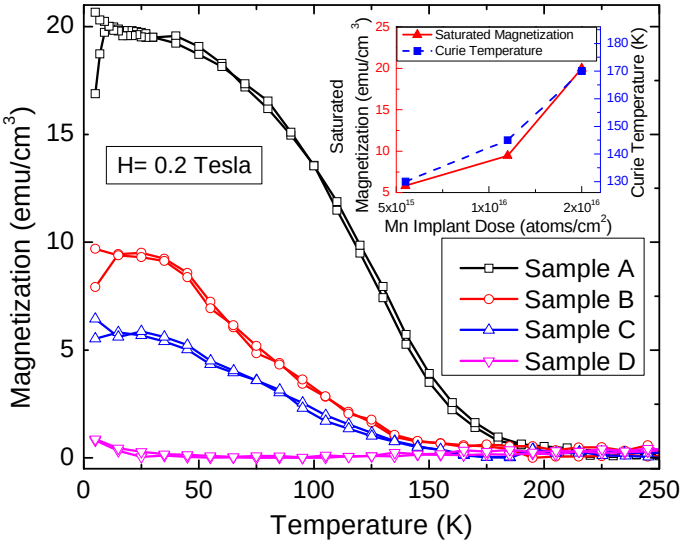


Figure 6.3: Temperature dependent in-plane saturated magnetization (at 0.2 Tesla) plot for four Mn-implanted epitaxial Ge samples. Each magnetization curve is made up of magnetic zero-field-cooled and field-cooled data. Inset shows that measured Curie temperatures and saturated magnetizations of Mn-implanted Ge samples scale monotonically with Mn implant dose [78].

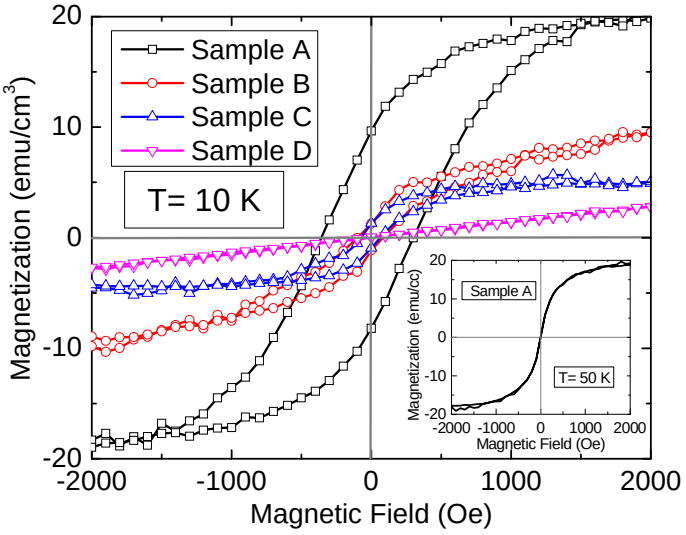


Figure 6.4: Magnetic hysteresis of four Mn-doped Ge samples at 10 K. The inset shows magnetic hysteresis of sample A at 50 K [78].

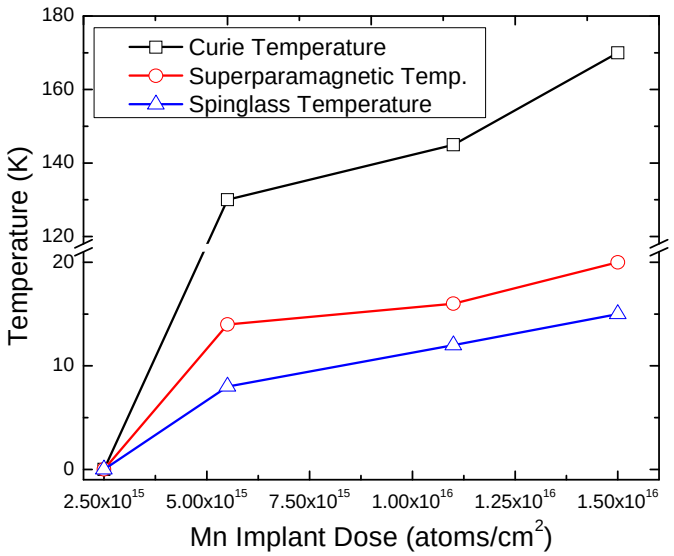


Figure 6.5: Basic phase diagram showing the dependence of Curie temperature, spin glass temperature and superparamagnetic temperature on total Mn-implant dose [78].

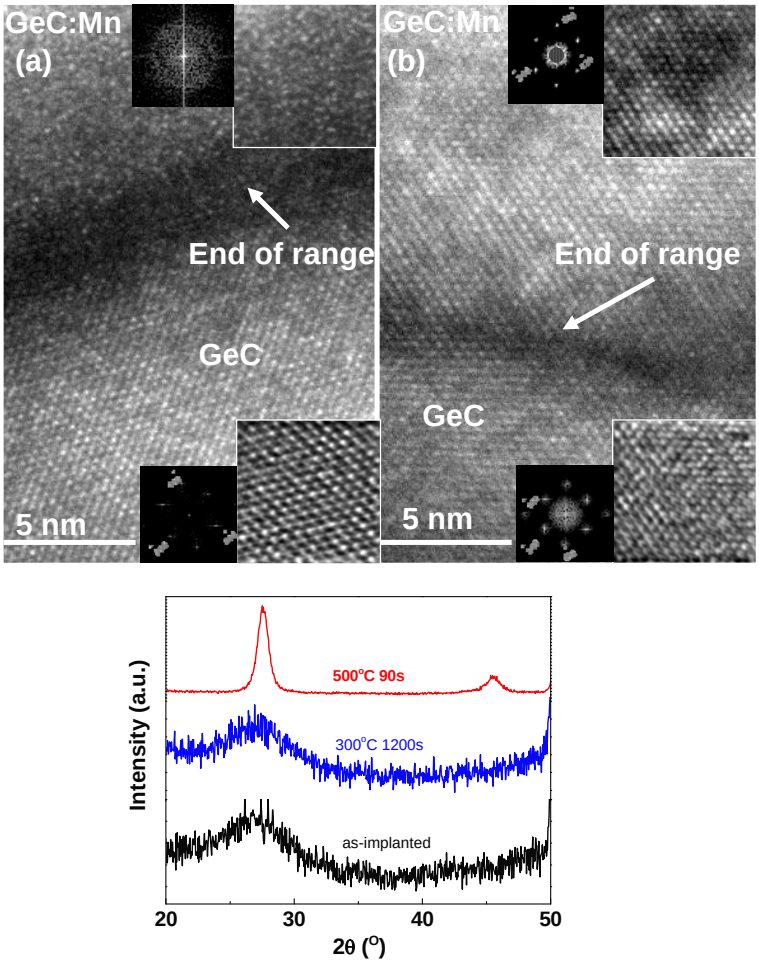


Figure 6.6: Transmission electron micrographs of sample A- (a) as-implanted and (b) annealed at 600°C for 90s with FFT and inverse FFT insets, (a) shows amorphous implanted region and crystalline Ge:C underlayer, and (b) the same sample annealed at 600ºC for 90s, showing a fully recrystallized region of Ge:C:Mn. Ferromagnetism in the sample is lost after recrystallization, indicating amorphous region contributes to the ferromagnetism [79]. (c) GI-XRD data ($\theta<\theta_{critical}$) of as-implanted and annealed samples show that recrystallization occurs during anneals performed at higher temperatures (> 300 °C).

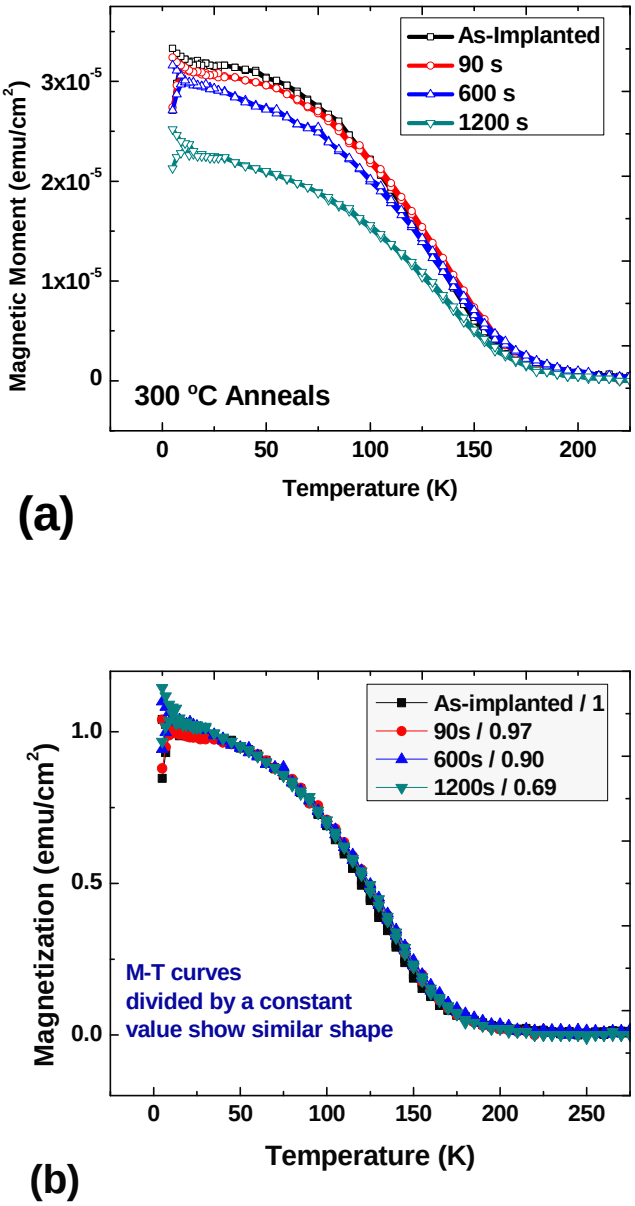


Figure 6.7: Temperature dependent in-plane saturated magnetization of sample A before and after annealing at 300°C for different durations. The inset shows normalized temperature-dependent magnetization plots for as-implanted and annealed (for different times) sample A [79].

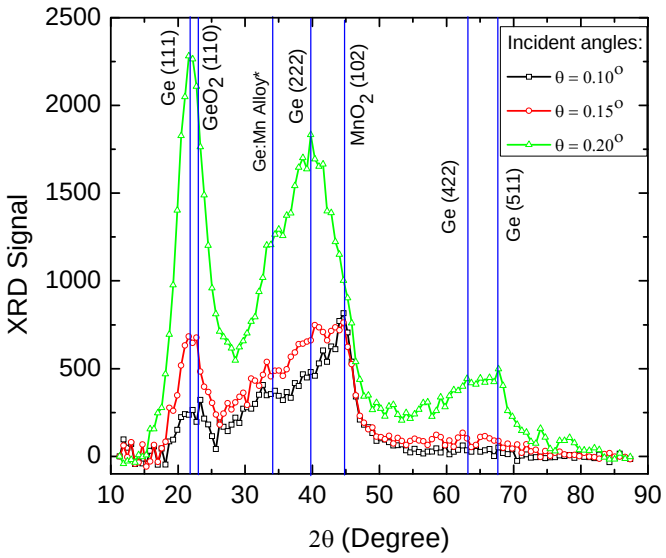


Figure 6.8: Synchrotron GI-XRD plot of sample A. (*This weak broad peak matches with highest peak of several Ge & Mn alloys: Ge_2Mn_5, Mn_2Ge, GeMn, $GeMn_3$, Ge_8Mn_{11} and Ge_3Mn_5.) [78].

Table 6.1: Summary of Mn-implant dose, Mn concentration, and magnetic properties of the Ge:C:Mn samples studied in this work [78].

Sample	Implanted Mn Dose	Peak Mn Conc.	Average Mn Conc.	Magnetic Property	T_C	Saturated Magnetization at 5 K, 0.2T	Superpara-magnetic Temp.	Spinglass Temp at 0.2 Tesla
Unit	cm^{-2}	at%	cm^{-3}		K	emu/cm^3	K	K
A	1.5×10^{16}	16	9.3×10^{21}	Ferro	170	20.0	20	15
B	1.1×10^{16}	12	7.5×10^{21}	Ferro	145	9.5	16	12
C	5.5×10^{15}	6	3.0×10^{21}	Ferro	130	5.9	14	8
D	2.5×10^{15}	2	7.8×10^{20}	Para, up to 5K	-	-	-	Not observed, up to 5 K

Chapter 7: Workfunction-engineered Ferro-magnet/Semiconductor Junctions for Efficient Spin Injection

We demonstrate a novel bilayer tunnel barrier to reduce contact resistance at the ferromagnetic-metal/semiconductor junctions for novel spin-devices. The proposed tunnel barrier consists of an ultrathin LaO_x/SiO_x stack which forms a dipole at the LaO_x/SiO_x interface and thus reduces the effective Schottky barrier height at the ferromagnetic-metal/semiconductor contact. The Co/n-Si contacts fabricated using LaO_x/SiO_x tunnel barriers demonstrate significant reduction (~0.3-0.5 eV) in Schottky barrier height and ~3-4 orders decrease in contact resistance, compared to the control Co/n-Si contacts fabricated using Al_2O_3 tunnel barriers. The optimized contacts with LaO_x(~1.2 nm)/SiO_x(0.6 nm) tunnel barrier demonstrate a low contact resistance of $\sim 3\times10^{-6}$ $\Omega.m^2$, which is close to the value required for efficient spin injection. Such reduction in contact resistance makes this technique a promising pathway for efficient spin injection/detection in future spin-based semiconductor devices.

7.1 INTRODUCTION

As the physical limits for scaling of conventional CMOS devices are on the horizon, novel scaling approaches including beyond CMOS spintronic devices are receiving interest [55]. Among these spintronic devices, spin-MOSFET fabricated using a semiconducting channel is one of the most promising approaches to integrate with contemporary CMOS devices [58]. Researchers all over the world are searching for a suitable semiconductor material with ferromagnetic properties (eg. Ga:Mn:As, Ge:Mn etc) to control the spin states in the channel or S/D of the proposed spin-MOSFETs [59,

60, 63, 78]. These ferromagnetic materials demonstrate many attractive properties, including carrier-mediated ferromagnetism [125]. However, in general, these materials are not suitable for device fabrication because of their low Curie temperature (T_C << 300K) [59, 78, 120]. One potential alternative to these low T_C materials is to fabricate the S/D regions using ferromagnetic metals (FM) with intrinsically high T_c (>700K). Then again, all the FM (Co, Fe, Ni, and alloys thereof) have a high workfunction (WF>5 eV) and hence show a high contact resistance (R_c) between the semiconducting channel and the metal. Such a high R_c is not suitable for efficient spin injection or detection in devices with conventional FM/semiconductor junctions. Although silicidation may result in a low R_c, this is not a solution to achieve efficient spin injection as the spin states get easily randomized in the silicided region [70]. In order to prevent silicidation, several insulators (I) have been introduced as tunnel barriers between FM/semiconductor contacts. Spin-injection form metal to semiconductor through these tunnel barriers has also been demonstrated. However, in general, operating temperatures of these devices are still very low (<<300K) which is to a large extent can be attributed to the R_c mis-match [69, 70]. In the case of n-Si, the R_c is much higher than the ideal value due to the workfunction mismatch between FM and conduction band. Although p-type Si may provide lower R_c because of the lower SBH with FM, they are not preferred for spintronic devices as spin-relaxation time is much shorter in p-Si because of the stronger spin-orbit coupling in the valence band than in the conduction band [72]. Recently, Min et al. have realized the low R_c required for efficient spin injection in $Ni_{0.80}Fe_{0.20}/Al_2O_3$/n-Si junctions using thin layers of low workfunction FM, namely Gd. However, this approach is again not suitable for pragmatic device applications, as Curie temperature of Gd is only 293K [126]. Therefore, we propose a novel tunnel barrier formed using a bilayer of oxides to reduce the effective Schottky barrier height (SBH) between the FM and n-type semiconductor

and hence to reduce the R_c for efficient spin-injection. In this work, we introduce a thin tunnel barrier consisting of an LaO_x/SiO_x bilayer that creates a dipole at the LaO_x/SiO_x interface (Figure 7.1(a)) [127] . The electric field caused by this dipole results in a band-bending within the tunnel barrier, which is favorable to reduce the effective workfunction of the metal relative to an n-type semiconductor and hence are widely used in the gate stack of high-k/metal-gate nMOSFETs to tune the workfunction of the metal to be close to the conduction band edge [127, 128]. Such reduction in effective SBH is also expected to reduce the R_c in FM/n-Si junctions, if an ultrathin LaO_x/SiO_x tunnel barrier is used. Recently, Sematech International has explored this technique of dielectric dipole mitigation (DDM) to fabricate low resistance contacts for nMOSFETs and has demonstrated low R_c contacts to n-Si using mid-gap workfunction metal, namely TaN [129].

In this work, we investigate the proposed concept of SBH modulation for spin-diodes using $Co/LaO_x/SiO_x$/n-Si junctions with different LaO_x thickness, where we have chosen Co as a FM for its high spin polarizibility [130] and Si as the semiconductor for its larger spin-diffusion length because of smaller atomic number and inversion symmetry of the crystal structure [68]. The control devices were fabricated with Al_2O_3, a conventional choice to fabricate tunnel barrier in spin-diodes. The junctions studied here were fabricated at and in collaboration with Sematech International. The author is indebted to Dr. Swaroop Ganguly for his guidance on this project, and is also thankful to Dr. Wei-yip Loh for his suggestions on design of experiment. The effects of LaO_x/SiO_x tunnel barrier on SBH and on R_c have been investigated from the evolution of junction I-V characteristics as a function of LaO_x thickness. The optimized LaO_x/SiO_x barrier results in a large decrease in SBH (~0.3-0.5 eV) and in R_c (~3-4 orders of magnitude), over the

control AlO_x barrier and hence demonstrate the efficacy of this approach to modulate SBH and R_c for efficient spin injection.

7.2 EXPERIMENTAL METHODS

Figure 7.1(b) shows the cross-sectional structure of the FM/I/S stack used in this work. Unless otherwise stated, moderately n-type (~1×10^{18} cm^{-3}) 200 mm Si wafers were used as the starting substrates. After standard cleaning, ultra-thin (~0.6 nm) SiO_x layers were deposited using an atomic layer deposition system. The LaO_x (0.8-1.6 nm) layers were deposited via sputtering from a La_2O_3 target, followed by in situ deposition of ~10 nm Co as the ferro-magnetic metal. The FM layer was capped in situ by ~20 nm Ta and ~100 nm TaN to prevent oxidation of the FM layer. Here the thin Ta barrier layer was used to prevent nitridation of the thin ferro-magnetic layer during TaN deposition. It may also be noted that La-based oxides are extremely hygroscopic and hence, it is mandatory to cap the LaO_x layer in situ to maintain the integrity of the stack and to obtain the expected behavior from these junctions. The FM/I/S diodes were defined via optical lithography, followed by TaN/Ta etching through reactive ion etching (RIE) using CF_4 plasma and Co etching using a diluted (10:1) HNO_3 solution. After removal of backside oxide, Al was deposited via DC sputtering to reduce the series resistance of the junctions.

7.3 RESULTS AND DISCUSSIONS

In order to extract the Schottky barrier height and contact-resistance of the spin-diodes, we have measured the I-V characteristics between the top and the bottom contact of the fabricated spin-diodes. The I-V characteristics of the spin-diodes clearly demonstrate the benefits of the LaO_x/SiO_x tunnel barrier over the AlO_x tunnel barrier. The reverse saturation current in the Co/n-Si (~$1\times10^{18}cm^{-3}$) junctions improve by more

than two orders of magnitude when only about 0.8nm LaO_x layer is used, along with ~0.7 nm SiO_x layer. The reverse saturation current increases further with increasing LaO_x thickness (up to ~1.2 nm), as the efficacy of this Schottky barrier modulation technique also increases with the improved uniformity in the deposited LaO_x layer. However, the reverse current increases again if thicker (>1.2 nm) LaO_x barrier is used, presumably due to increased tunneling resistance. In Figure 7.2 (b), we have estimated the SBH (using I-V method) of the same spin-diodes, which show that the SBH decreases with increasing LaO_x thickness and saturates for LaO_x thickness > 1.2 nm. Therefore, it appears, the optimum LaO_x thickness to reduce SBH in the Co/n-Si systems investigated is ~1.2 nm.

Next, to investigate the effects of such Schottky barrier modulation on contact resistance, we have estimated the contact resistances of these spin-diodes from the slope of the I-V characteristics at a forward bias of 0V. As expected, Figure 7.3 (a) shows that the proposed bilayer LaO_x/SiO_x tunnel barrier decreases the R_c by ~4 orders of magnitude, over the control Al_2O_3 tunnel barrier. The contact resistance of the junctions as a function of LaO_x thickness shown in Figure 7.3(a) exhibit a U-shaped curve, where 1.2 nm LaO_x results in the lowest R_c. Initially, R_c decreases due to SBH modulation due to dipole formation and may also be due to improved passivation, then the R_c increases again due to increased contribution from tunneling resistance. We hypothesize that further process development to deposit the LaO_x/SiO_x tunnel barrier more uniformly may result in even lower R_c with thinner tunnel barriers. Nevertheless, the minimum R_c (~3×10^{-6} Ω-m^2) achieved in this work is one of the best reported in literature for FM/I/S contacts, especially on such moderately doped n-Si (~$1\times10^{18}cm^{-3}$) substrates. Furthermore, the lowest R_c achieved in our devices is close to the ideal R_c required for efficient spin injection into n-Si with such doping density (as shown by the dotted line in Figure 7.3 (a)). For comparison, we have adapted the required R_c vs. doping density plot

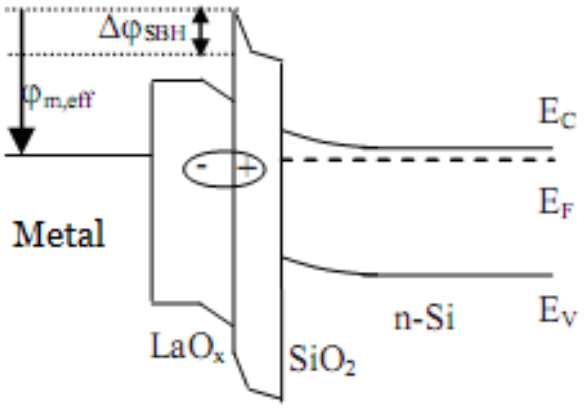
from [69] in Figure 7.3 (b) , which show that the high R_c observed in our Co/AlO_x/n-Si junctions are expected on the substrates with this doping density. Figure 7.3(b) further shows that LaO_x/SiO_x bilayer lowers the R_c by ~10^4 times, which is very close to the R_c required for efficient spin injection/detection on n-Si substrates, irrespective of the doping density. However, the R_c needs to be further reduced to reach the ideal condition for efficient spin injection, specially at room-temperature. We also observed similar reduction (~4 orders of magnitude) in R_c when lightly-doped n-Si substrates are used (Figure 7.3 (b)). Although the absolute value of R_c is much higher on lightly-doped substrates, the requirement for R_c is less-stringent on them because of the larger spin-diffusion length at lower doping densities.

In order to extract the SBH of these Co/n-Si junctions more accurately, we have measured the I-V characteristics of the spin-diodes at elevated temperatures (300K-370K), and fitted the I_{OFF} data (at reverse bias) in Arrhenius plots. For instance, in Figure 7.4 (a), we show the temperature-dependent I-V characteristics of Co/LaO_x(~1.2 nm)/SiO_x/n-Si(~$1\times10^{15}$$cm^{-3}$) spin-diodes, while the Arrhenius plot derived from the same data is shown in Figure 7.4 (b). We have extracted an SBH of ~0.4 eV between Co and the Si substrate, from the slope of this Arrhenius plot (0.34) and the ideality factor of the spin-diodes (n ~1.45). It may be noted that the ideality factor of these diodes are fairly high (>1), which is not unexpected for such M/I/S junctions because of the contribution from large resistive component, namely the insulating tunnel barrier. We summarize the SBH data extracted using the above mentioned temperature-dependent method in Figure 7.5, which further confirms the suitability of the LaO_x/SiO_x tunnel barrier as an R_c reduction technique for efficient spin injection into n-type semiconductors.

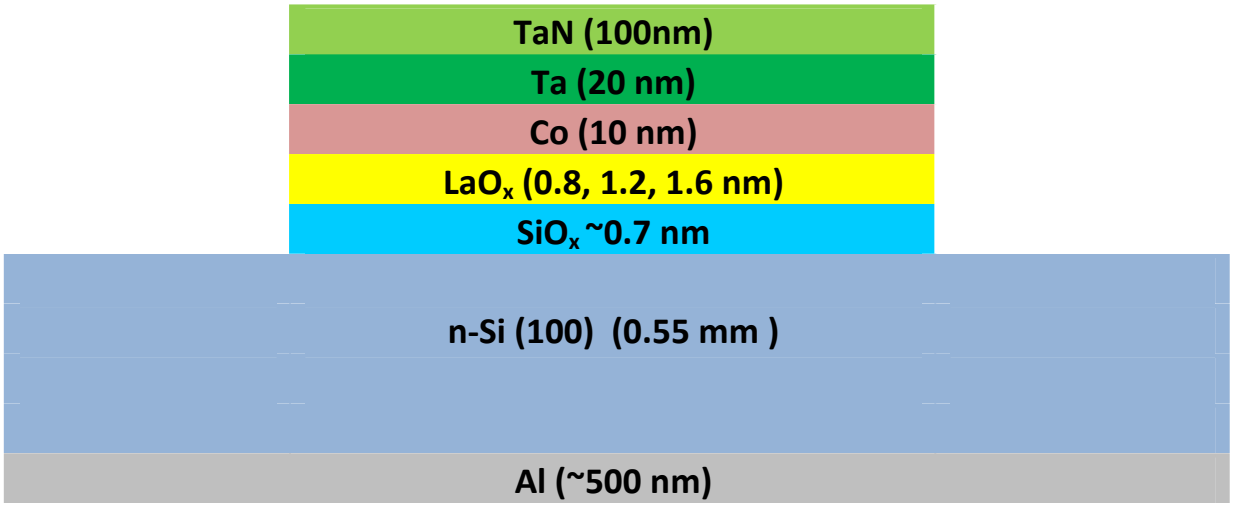
The low R_c achieved using LaO_x/SiO_x dual barrier makes it a promising candidate to fabricate tunnel barriers for efficient spin injection into semiconductors. However, spin injection/detection into Si using this LaO_x/SiO_x barrier is yet to be demonstrated. Furthermore, it may be noted that, in addition to optimum R_c, ideal tunnel barriers are also expected to provide spin filtering effect for more efficient spin injection and to have higher polarization. In this context, the properties of conventional single layer tunnel barriers (eg. Al_2O_3, MgO, SiO_2 etc.), used in contemporary Si spintronic devices are discussed in appendix B.

7.4 SUMMARY

In summary we demonstrate a simple approach to reduce the contact resistance in FM/semiconductor spin-diodes by using a bilayer tunnel barrier formed by a thin LaO_x/SiO_x stack. A dipole is formed at the LaO_x/SiO_x interface that reduces the effective Schottky barrier height at Co/n-Si contacts by ~0.3-0.5 eV compared to the control diodes with AlO_x tunnel barrier. The reduced Schottky barrier reduces the R_c in FM/I/S contacts by ~4 orders of magnitude, compared to the control devices. The lowest R_c achieved using $Co/LaO_x/SiO_x$/n-Si contacts is $\sim 3\times10^{-6}$ Ω-m^2, which makes it a promising pathway for efficient spin-injection/detection in potential novel spintronic devices.



(a)



(b)

Figure 7.1: (a) Band-diagram illustrating the high-k dipole at the LaO_x/SiO_x tunnel barriers in M/I/S junctions (adapted from [131]); (b) Cross-sectional schematic of the FM/I/S junctions investigated.

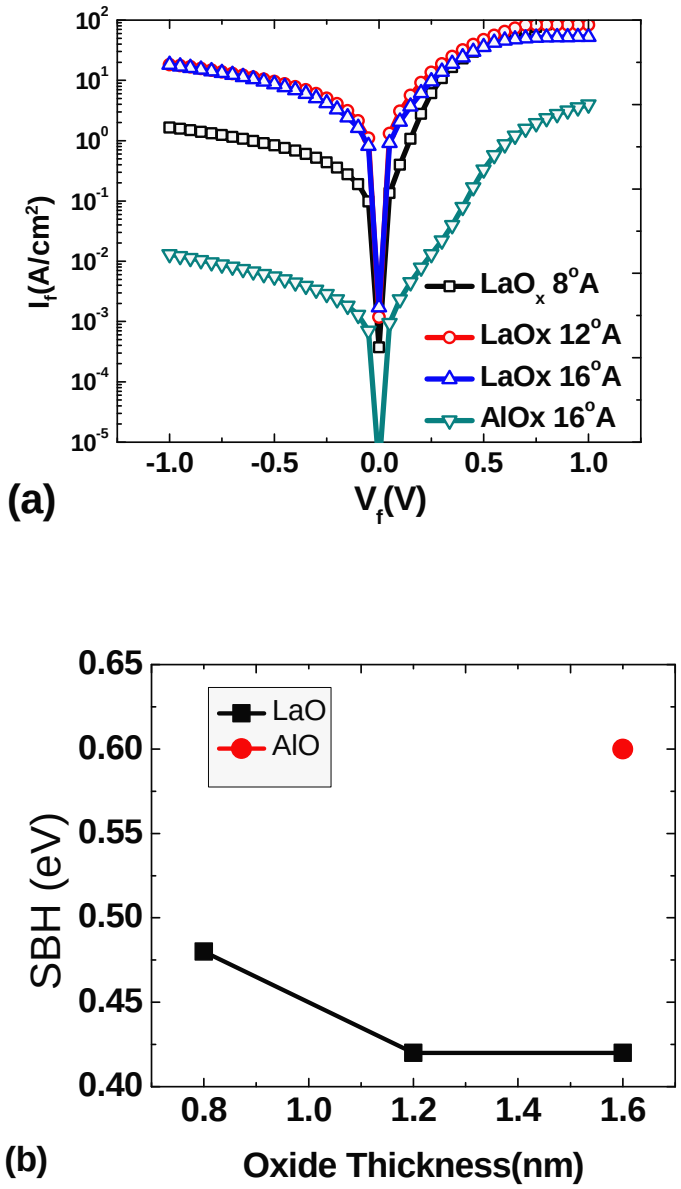
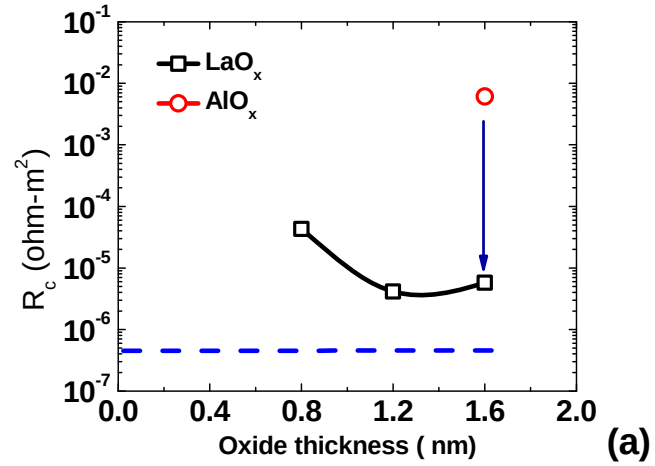


Figure 7.2: (a) LaO_x/SiO_x tunnel barrier shows increase in reverse current, compared to the control AlO_x/SiO_x tunnel barriers, indicating reduced effective Schottky barrier height (SBH); (b) SBH (extracted using I-V method) between Co and n-Si goes down when LaO_x/SiO_x tunnel barriers are used, however, reduction in SBH saturates for LaO_x thickness >1nm.



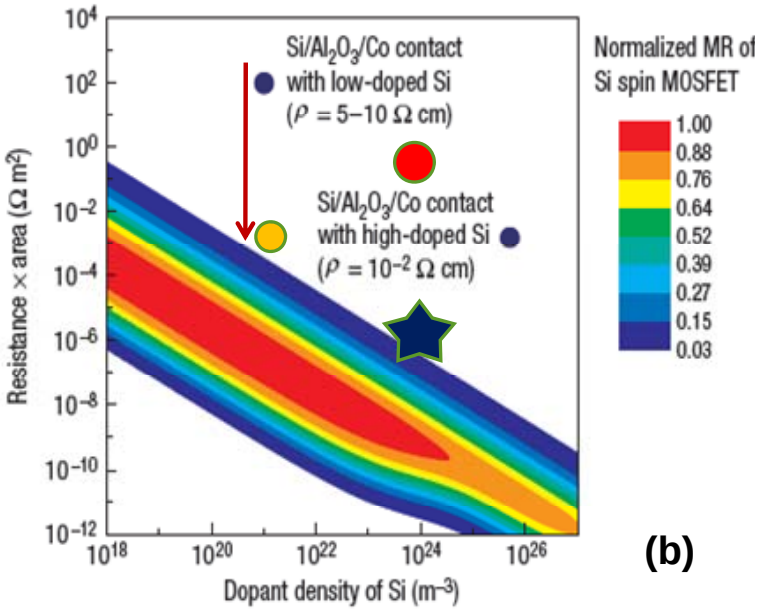


Figure 7.3: (a) LaO_x/SiO_x tunnel barrier shows decrease in contact resistance with increasing LaO_x thickness (for up to ~1nm) for better SBH modulation; Thicker LaO_x (>~1nm) increases the contact resistance again due to increased tunneling resistance; (b) The reduction in R_c is similar for different substrate doping densities and the achieved R_c is very close to the condition required for spin-injection into n-Si (R_c vs. doping density plot adapted from [69]).

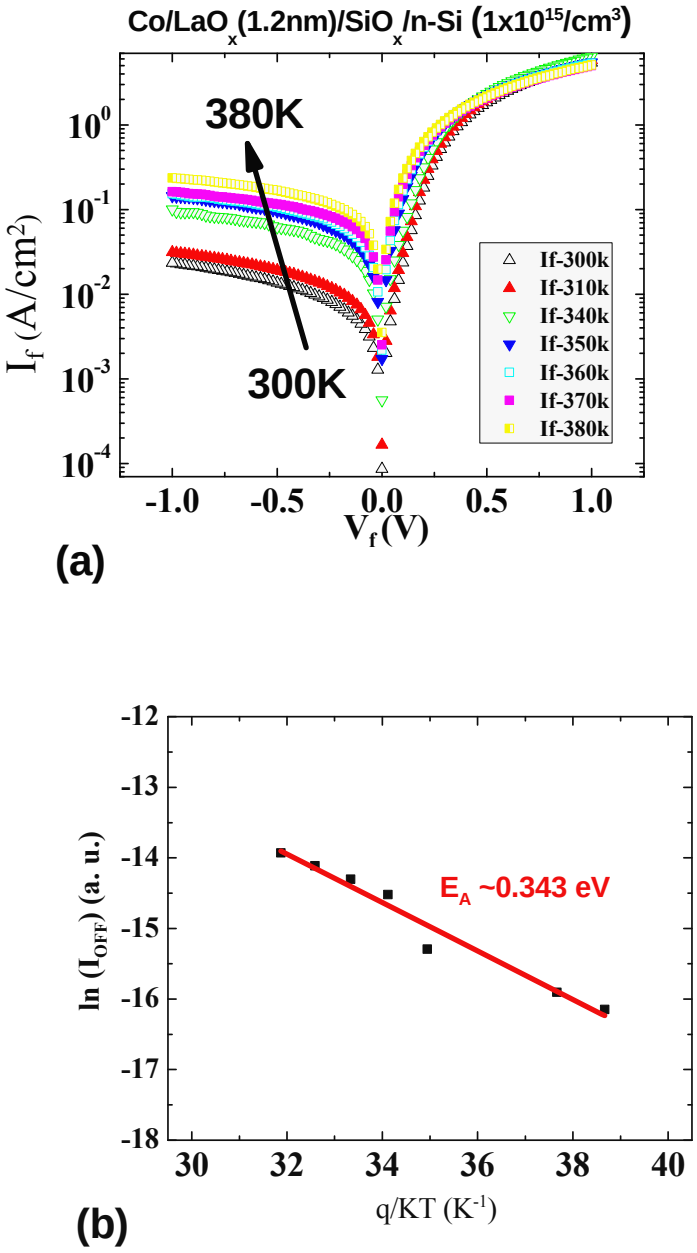


Figure 7.4: (a) Temperature-dependent I-V characteristics of Co/LaO_x(1.2 nm)/SiO_x/n-Si(~1×10^{15} cm^{-3}) junctions. (b) Arrhenius plot of I_{OFF} extracted from the I-V characteristics shown in (a); The Arrhenius plot shows a slope of 0.34 eV that corresponds to an SBH of ~0.4 eV, whereas, SBH extracted using the same method from Co/AlO_x/n-Si contacts is ~0.9 eV.

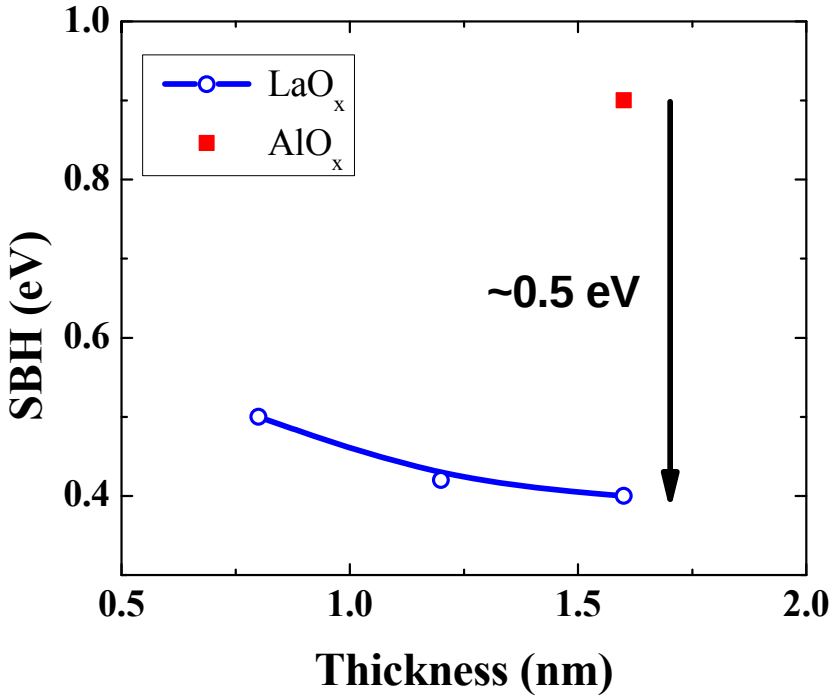


Figure 7.5: SBH extracted from temperature-dependent I-V characteristics of the Co/I/n-Si diodes; effective SBH decreases for increasing LaO_x thickness. O the other-hand conventional Al_2O_3 tunnel barrier shows a high SBH of 0.9 eV, which is 5 orders of magnitude higher than the lowest SBH achieved using LaO_x/SiO_x bilayer.

Table 7.1 Split matrix for FM/I//n-Si junctions studied in this work

Sample #	**Starting Substrate**	**Oxide 1 (nm)**	**LaO_x (nm)**
1	n-Si ($1\times10^{18}/cm^3$)	**Al_2O_3 – (1.6)**	**0**
2	n-Si ($1\times10^{15}/cm^3$)	SiO_x – (0.7)	**1.2**
3	n-Si ($1\times10^{18}/cm^3$)	SiO_x – (0.7)	**0.8**
4	n-Si ($1\times10^{18}/cm^3$)	SiO_x – (0.7)	**1.2**
5	n-Si ($1\times10^{18}/cm^3$)	SiO_x – (0.7)	**1.6**

Chapter 8: Summary and Future Work

8.1 SUMMARY OF THE THESIS

In this work a few synergistic approaches have been proposed to circumvent the challenges towards fabrication of high-performance Ge-based CMOS devices and beyond. Chapter 2 simultaneously addressed the issues of bulk Ge and surface passivation, by fabricating Si-capped Ge:C pMOSFETs on epitaxial Ge:C-on-Si substrates. Epitaxial Ge:C provides lower defect density than epitaxial Ge grown on Si substrates, while Si capping prevents GeO_x formation and passivates the Ge:C surface. In addition, the quantum well for holes formed in the Si/Ge:C/Si structure reduces remote Coulomb scattering and enhances the pMOSFET performance. The effects of Si cap thickness (3 to 9 nm) on these Ge:C devices have been investigated via temperature-dependent electrical characterization, along with device simulations. The study identifies the routes to optimize device design for epitaxial buried channel Ge-channel pMOSFETs.

Chapter 3 demonstrated a simple route to passivate Ge surface using a thin GeO_2 passivation layer grown by rapid thermal oxidation (RTO) and investigated the thermal stability of the GeO_2-passivation for MOS device applications via electrical and material characterization. The RTO-passivated MOSCAPs show improved electrical characteristics over the MOSCAPs without RTO. The improved passivation results in ~1.8× enhancement in μ_{eff} in RTO-passivated Ge (100) pMOSFETs over their HF-last counterparts. Germanium (111) pMOSFETs with RTO-passivation show a high μ_{eff} of ~270 $cm^2V^{-1}s^{-1}$ (at E_{eff}~0.2 MV/cm), demonstrating ~2× enhancement over universal Si/SiO_2 mobility. The Ge nMOSFETs fabricated using the RTO-grown passivation layer on higher mobility (111) orientation show a high μ_{eff} of ~713 $cm^2V^{-1}s^{-1}$ (at the peak) and

thus the MOSFETs fabricated demonstrate suitability of this RTO-passivation approach to achieve Ge CMOS devices with high electron mobility.

In chapter 4, we investigated the reasons for underperformance of Ge nMOSFETs via temperature-dependent and pulsed I-V characterization. Temperature-dependent characteristics suggest that despite significant improvement over HF-last devices and a low D_{it} near the mid-gap, the GeO_2-passivated devices still suffer from remote Coulomb scattering. Besides, the ns pulsed I-V characterization suggests significant charge trapping in the gate dielectric. In addition, these devices also suffer from low activation of n-type dopants, and a high density of implantation-induced defects in the S/D junctions, which also significantly contribute to the underperformance of these Ge nMOSFETs.

Chapter 5 demonstrated a simple approach to form high performance n^+/p junctions in Ge by rapid thermal diffusion of P from "Spin-on Dopants" (SOD) that avoids implantation damage. The junctions formed using this approach show a high I_{ON}/I_{OFF} ratio ($\sim 10^{5\text{-}6}$) and an ideality factor of ~1.03, indicating a low defect density. Furthermore, Ge (100) and (111) nMOSFETs were fabricated with these SOD-doped junctions and a thin RTO-grown passivation layer in the gate stack to integrate the benefits of low D_{it} at the Ge/GeO_2 interface with the low defect density of the SOD-doped junctions.

In chapter 6, we investigated Ge:C:Mn thin films grown on Si as a ferromagnetic material for spintronic devices which is promising for a long-term potential alternative to contemporary CMOS devices. The Ge:C:Mn thin film was formed by low energy ion implantation of Mn^+ on epitaxial Ge:C-on-Si substrates to utilize their Si compatibility. The evolution of magnetic properties with Mn concentration and crystalline structure has been thoroughly investigated with a view to optimizing this novel material system.

In chapter 7 we proposed a novel tunnel barrier for spin-MOSFETs that is fabricated using LaO_x/SiO_x bilayer and can modulate the Schottky barrier height (SBH) at the ferromagnetic metal/n-Si junctions. Thus the effective SBH at the Co/n-Si junction is reduced by ~0.4-0.5 eV and thus we have achieved ~4 orders of magnitude reduction in contact resistance (R_c), which is favorable for spin injection into n-type semiconductors. The low R_c ($\sim 3\times10^{-6}$ $\Omega.cm^2$) achieved in this work show promise for potential use in future spintronic devices.

8.2 FUTURE WORK

8.2.1 Future experiments for Ge CMOS applications

The high mobility Ge nMOSFETs demonstrated in this work and in several other recent reports are fabricated on bulk Ge wafers that are not suitable for high volume CMOS production. Therefore, the RTO-grown GeO_2 passivation and SOD-based diffusion doping technique proposed in this work need to be optimized on epitaxial Ge substrates, especially on Ge:C-on-Si thin films to take the advantage of their Si compatibility, while maintaining a lower defect density. Besides, the RTO-grown GeO_2 tunnel barrier may be introduced at the metal/n-Ge contact to reduce metal-induced gap states and hence to reduce contact resistance. Usage of an ultra-thin tunnel barrier with minimal conduction-band offset (namely Ta_2O_5) may be more effective for this purpose.

Growth of epitaxial Ge on Si(111) substrates should be interesting to take the advantage of higher electron mobility on (111) orientation. As shown in Figure 8.1, initial experiments show that addition of trace amount of C results in a smoother Ge layer grown on Si(111). The better crystalline quality of Ge:C/Si(111) over Ge (111)/Si(111) is more evident from the X-TEM images (Figure 8.2). Similarly, integration of higher hole

mobility (110) orientation for pMOSFET applications would provide even higher hole mobility. However, it may be noted that Ge films grown on (111) and (110) orientations are more prone to formation of threading dislocations. This is also supported by the initial experiments on Ge:C/Si(111), which showed higher rms roughness (~1 nm) than that of Ge:C/Si (100) (~0.35 nm). Fabrication of Ge-on-Insulator substrates with Ge (111) device layer may be a promising alternative and more suitable for IC industry, as it is expected provide better electro-static control and may also avert the challenge of cleaving (111) wafers into regular rectangular shapes. Finally, fabrication of FINFETs with (111) sidewalls may provide another attractive pathway to make high mobility Ge (111) surface suitable for high volume CMOS production.

In addition, Ge nMOSFETs demonstrated so far are fairly long channel, and hence, fabrication of short-channel (sub-100 nm) devices will provide us with useful insights about their scalability. We hypothesize that highly scaled (width ~10 nm) Ge nanowire MOSFETs may be interesting as the channel formed by volume inversion would be less sensitive to the surface states, which significantly limit the performance of Ge-based devices. It may be noted that the diffusion doping technique proposed in this work is not readily transferrable for short-channel devices because of large lateral diffusion. Newly proposed monolayer doping [132] or co-implantation [114] technique may be introduced to enhance activation, and to reduce junction-depth by avoiding or reducing implantation damage. As shown in Figure 8.3, initial experiments of Sb and P co-implantation performed on bulk Ge wafers demonstrate nearly ideal junction characteristics with a low I_{OFF}, thanks to the low defect density achieved by strain-compensation. Further optimization of this technique for short-channel epitaxial MOSFETs would be a major boost for Ge-based device technology.

In order to circumvent the shortcomings of Ge n^+/p junctions, we also propose fabrication of Ge nMOSFETs with Si or SiGe S/D junctions (Figure 8.4). In addition to the higher solubility and lower diffusion of n-type dopants in them, Si or SiGe S/D junctions are also expected to apply tensile strain in the Ge channel and hence to increase the electron mobility even more. Usage of Ge-on-Ge:C/Si as a channel material may be beneficial for low defect density and strain relaxation due to segregated C atoms at the interface, as compressive strain is detrimental for electron mobility [133]. It may be noted that lower thermal budget of Ge, especially for epitaxial films and at the gate stack, requires significant process development for realization of the proposed structure. For instance, development of a channel-last MOSFET flow or selective deposition of highly doped Si or SiGe at low temperatures will be required to achieve the expected performance from the proposed MOSFET structure.

Finally, in Figure 8.5, we have summarized the approaches proposed in this work for high performance Ge nMOSFET fabrication.

8.2.2 Future experiments for beyond CMOS applications

In chapter 7, we have investigated Ge:C:Mn thin films on Si as a ferromagnetic material for S/D or channel regions of Spin-MOSFETs. Despite its Si compatibility the material is not suitable for realistic devices because of its low T_c (<180K). As discussed in chapter 8, one potential alternative is to use ferromagnetic metals (FM) with intrinsically high T_c (>700K) as the S/D of Spin-MOSFETs along with LaO_x/SiO_x tunnel barriers for Schottky barrier height (SBH) modulation to achieve lower contact resistance (R_c). The initial experiments show promise of the proposed technique by reducing the workfunction (WF) by ~0.3-0.5eV that reduces R_c by ~4-5 orders of magnitude in

$Co/LaO_x/SiO_x/n$-Si junctions over $Co/Al_2O_3/n$-Si junctions. However, additional 2-3 orders of reduction in R_c is required for efficient spin-injection [69]. As shown in [134] and in Figure 8.6(a), an SBH of ~0.25eV (another ~0.2eV decrease in SBH) is required to reduce R_c to an ideal value for efficient spin injection [69]. Therefore, we propose introduction of tensile-strained Si as a channel material for Spin-MOSFETs, which would provide additional ~0.2eV reduction in SBH by lowering the conduction band [135] (Figure 8.6(b)). Thus, strained-Si, in combination with LaO_x/SiO_x dual barrier, should reduce the R_c by another ~2-3 orders of magnitude, which is expected to provide efficient spin-injection into semiconductors and will facilitate realization of spin-MOSFETs with S/D contacts formed by conventional ferromagnetic metals.

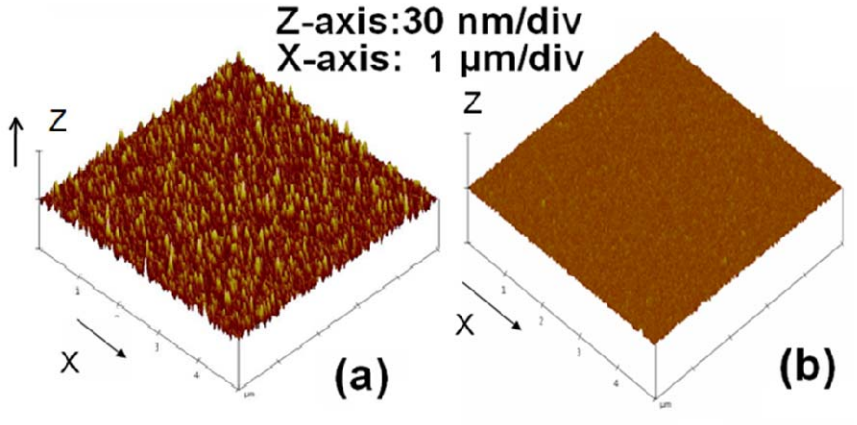


Figure 8.1: AFM surface images of: (a) Ge/Si(111) (RMS roughness ~2.0 nm) and (b) Ge:C/Si(111) (RMS roughness ~1.0 nm). Carbon incorporation results in a smoother surface.

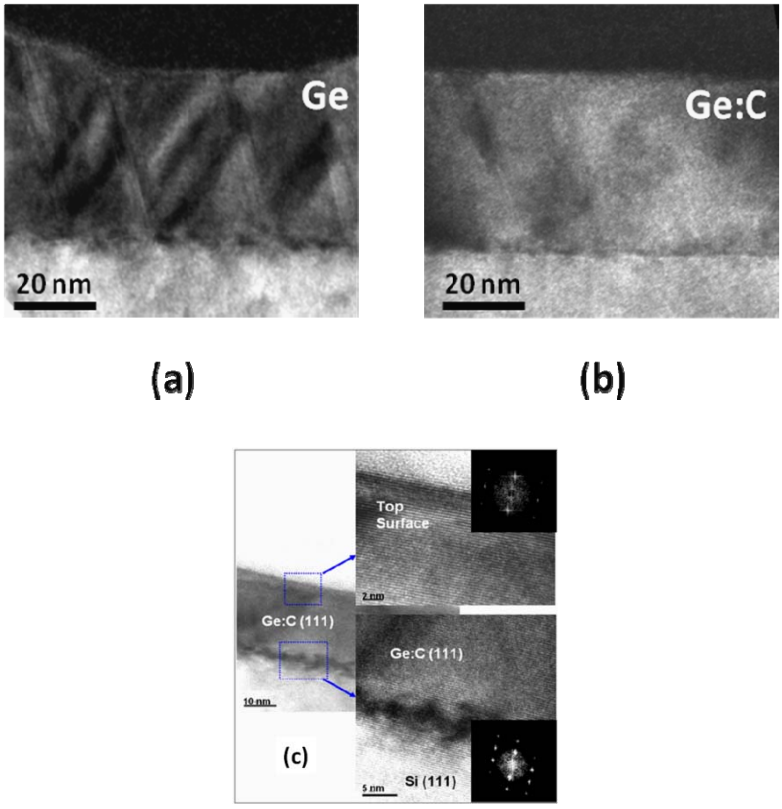


Figure 8.2 (a) and (b) shows dark field X-TEM images of Ge grown on Si(111) and (b) Ge:C grown on Si(111), respectively. The Ge:C(111) film shows fewer threading dislocations. (c) high resolution bright field X-TEM images near the top and bottom interface of the Ge:C/Si(111) which shows high crystalline quality in the top layer and higher concentration of misfit dislocations near the bottom interface.

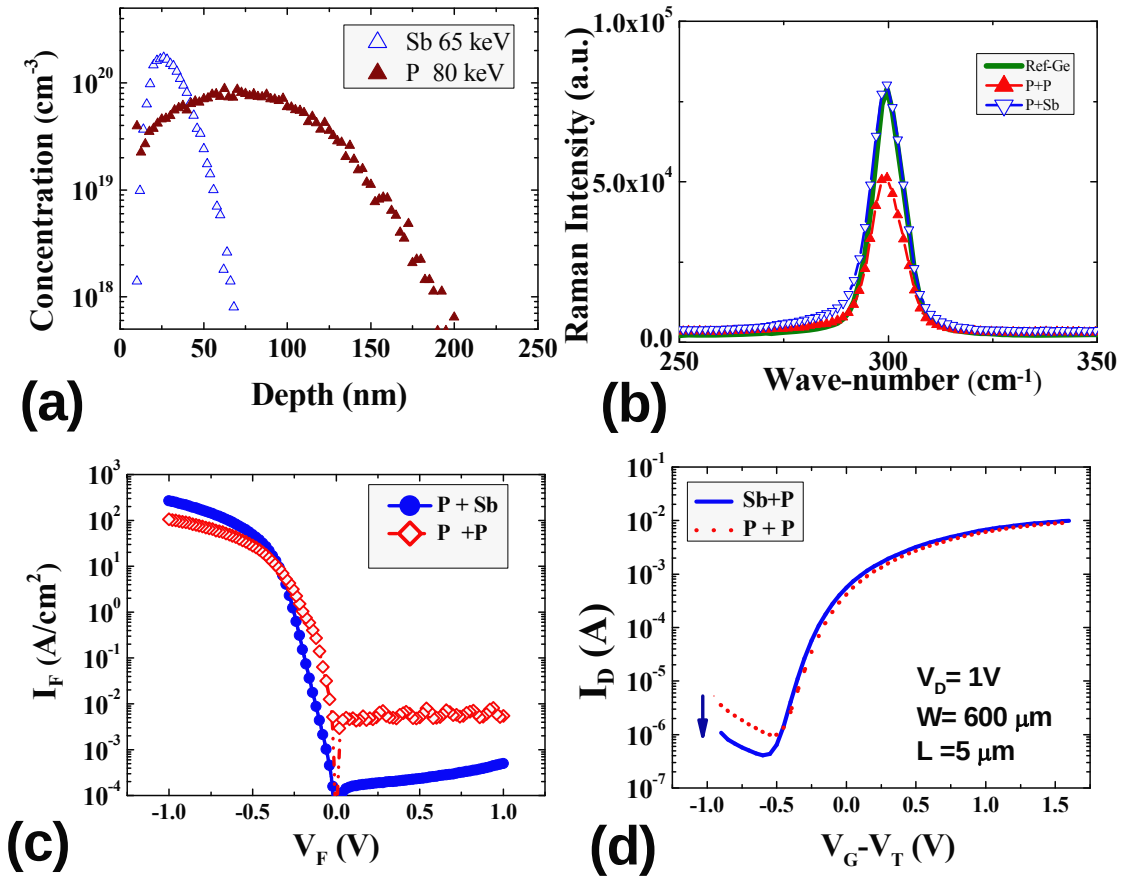


Figure 8.3: (a) SRIM simulation profile of as-implanted Sb and P in co-implanted sample. In control sample dual P implant was used to match the doping profile (b) after activation, co-implanted sample shows higher Raman intensity comparable to reference Ge, indicating better crystalline quality than that of the control sample (c) the improved crystalline quality results in better junctions in co-implanted samples with a high I_{ON}/I_{OFF} ratio of ~10^6 and a near unity ideality factor of 1.03 (d) Ge nMOSFETs with co-implanted junctions show lower I_{OFF} and higher I_{ON}.

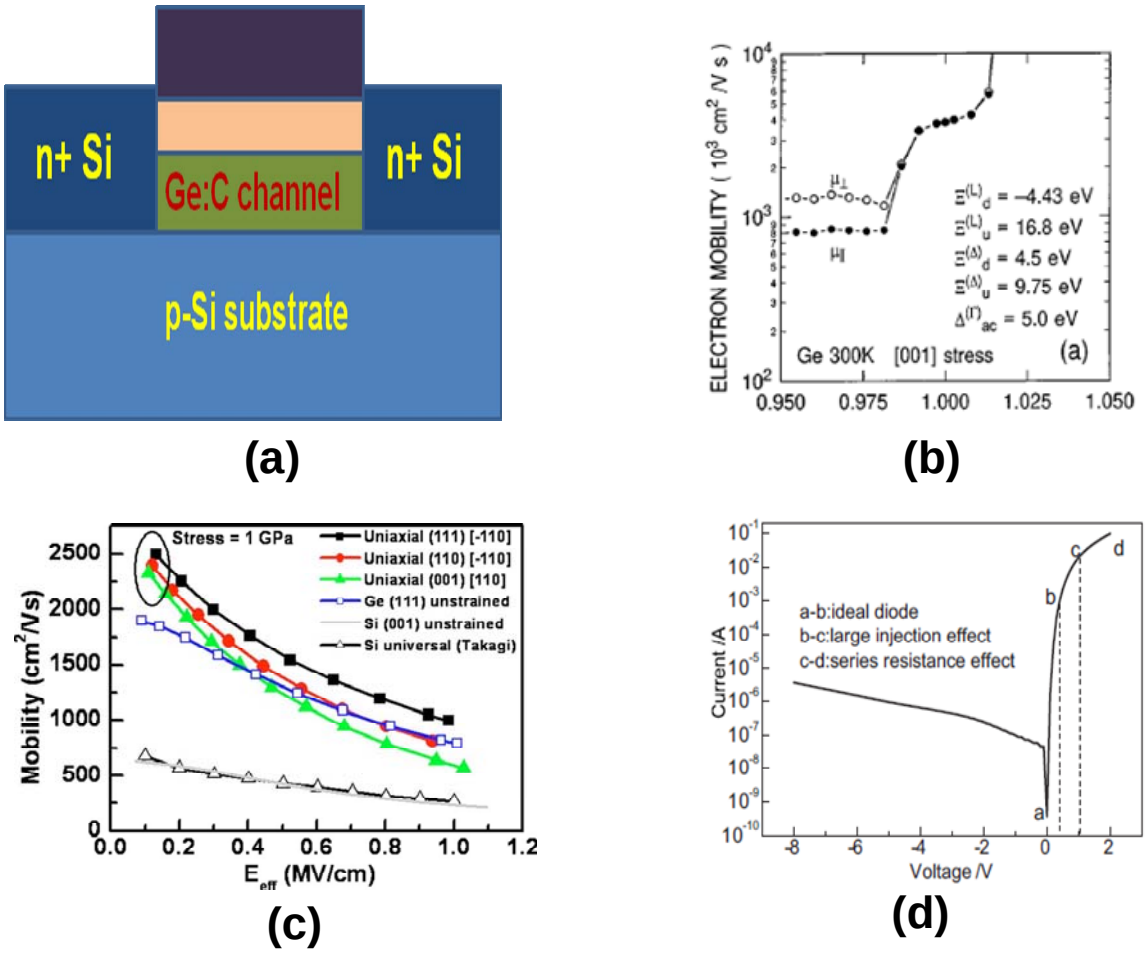


Figure 8.4 (a) proposed structure for Ge nMOSFET with Si (or SiGe) S/D regions, designed to improve n^+/p junction performance by utilizing higher solid solubility and lower diffusion of n-type dopants in Si (or SiGe). (b) Tensile-strained Ge is expected to show significant enhancement in electron mobility [133] (c) theoretical prediction also suggests enhancement in effective mobility in tensile-strained Ge nMOSFET, especially under uniaxial stress [96], and (d) i-Ge/n^+-Si diodes show a high I_{ON}/I_{OFF} ratio and a low I_{OFF}, demonstrating the benefit of higher n-type dopant activation and wider bandgap of Ge [136].

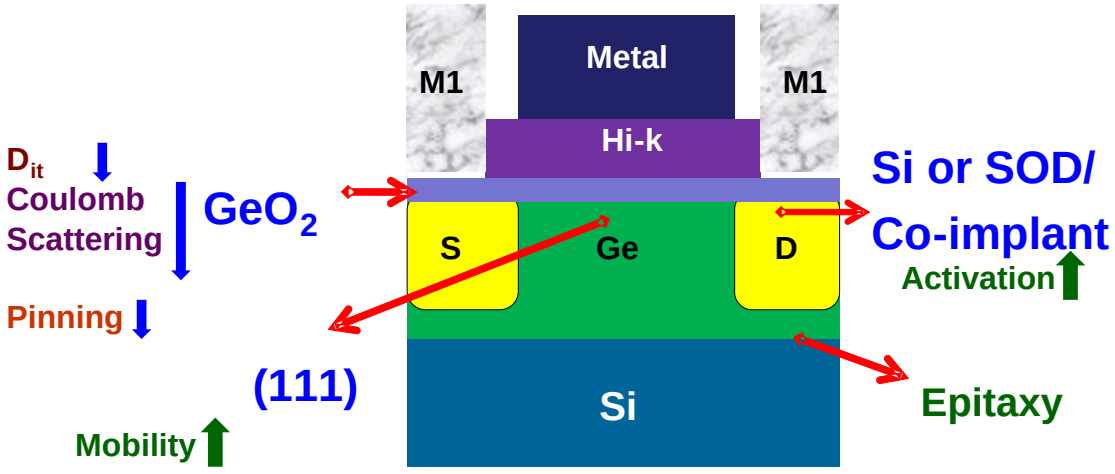


Figure 8.5: Conceptual schematic of the proposed Ge nMOSFET, showing the key opportunities to improve its performance.

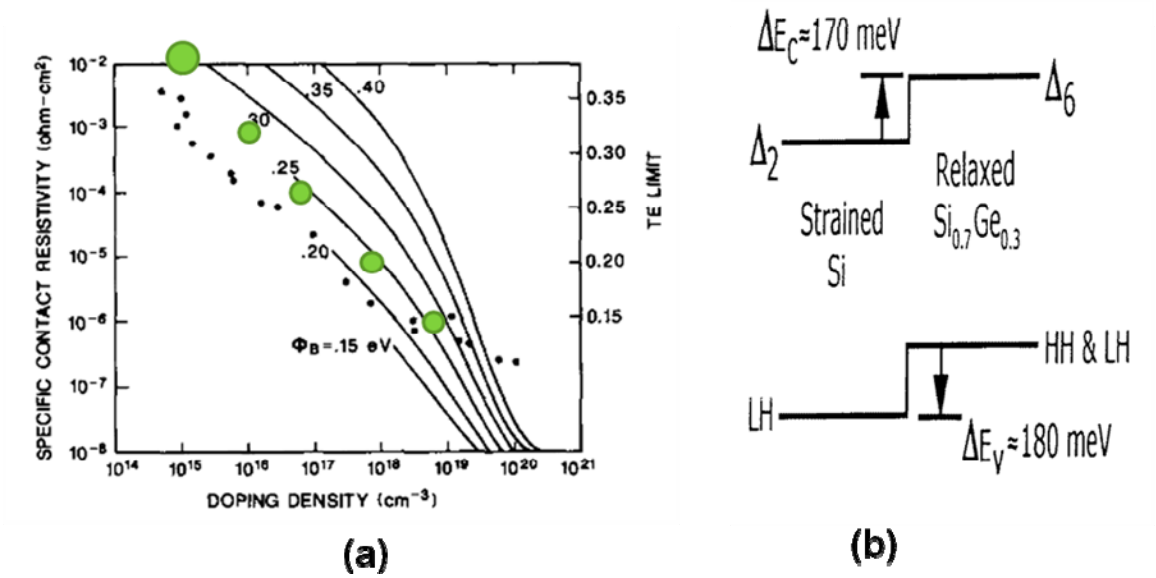


Figure 8.6: (a) A low SBH of ~0.25eV is required for the ideal R_c for efficient spin injection, as predicted in [69] (graphics adapted from[134]); (b) Usage of tensile Si instead of relaxed-Si is expected to provide additional ~0.2eV reduction in SBH, which in combination with LaO_x/SiO_x tunnel barrier would facilitate realization of ideal SBH of ~0.25eV, for efficient spin injection from FM to semiconductor.

Appendix A

Table A.1 Valence band offset at Si-Ge interfaces

s-Si, s-Ge : strained Si and Ge layer respectively.
ΔE_V : Valence band offset
$\Delta E_{V,\,AV}$: The offset of the uppermost three valence bands, is nearly independent of strain (and orientation), with a weak linear dependence on strain (lattice constant parallel to the interface) [137], [138].

Active/Substrate	**ΔE_V (eV)**	**$\Delta E_{V,AV}$ (eV)**	**Method**	**Reference**
s-Ge/Si	0.84	0.54	Local density functional + ab initio pseudopotentials	[137]
s-Si/Ge	0.31	0.51		
s-Ge/Si	0.74		[138] + Deformation potential theory to estimate bandgaps	[139]
s-Ge/Si	0.74		Pseudopotential empirical calculation	[137]
s-Si/Ge	0.22			
s-Ge/Si	0.74	0.45	Average bond energy theory + deformation potential method	[140]
s-Si/Ge	0.22	0.43		
Si/Ge	0.52	0.45		
s-Ge/Si	0.34, 0.49, 0.51		Yield Spectroscopy	[141]
Ge/Si	0.34, 0.35, 0.37			
s-Ge/Si	0.55, 0.61, 0.69		XPS	
Ge/Si	0.55, 57, 0.63			
s-Si/s-Ge on relaxed $Si_{0.5}Ge_{0.5}$	0.64		Experimental +Simulated CV	[142]
Si/Ge or Ge/Si	0.84		Ab initio natural band offsets	[143]
Ge/Si	0.59		k.p method	[144]

Appendix B

Table B.2 Comparison of different tunnel barriers used for spin injection

Barrier	Barrier Properties		R_c between FM/n-Si	Spin Life-time (ps)	Spin Diffusion Length (nm)	FM/Semiconductor (or M), Reference
	Filter Effects	Crystalline				
Al_2O_3	No	No	High to n-Si	107	204	NiFe/ p-Si, [145]
			Cs treatment lowers SBH by ~0.5 eV, ~ 1.5×10^{18} cm^{-3}	>150	–	NiFe/ n-Si, [146]
MgO	Yes	Yes	High to n-Si	276	328	NiFe/ p-Si, [145]
			6 kΩ.μm^2 n-Si ($1e^{20}cm^{-3}$)	9440 (at 8K)	2800 (at 8K)	Fe/ n-Si, [147]
			6 kΩ.μm^2 n-Si ($5e^{19}cm^{-3}$)	~5500 (at 100K)	~1550 (at 100K)	Fe/ n-Si, [148]
SiO_2	No		~1.2 kΩ.μm^2 n-Si (~3×10^{18} cm^{-3})	320 (at 10K)	400 (at 300k)	Co-Fe/ n-Si, [149]
$LaAlO_3$	No	Both crystalline and amorphous	-	Spin polarization of ~77% , at 4K		LSMO/ LSMO, [150]

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